INTERNATIONAL JOURNAL OF MICROWAVE AND OPTICAL TECHNOLOGY,
VOL.9, NO.1, JANUARY 2014

Inverse Class-F Power Amplifier Using Slot Resonators as a Harmonic Filter

Yu.V. Rassokhina[1], V. G. Krizhanovski[1], P. Colantonio[2] and R. Giofrè[2]

[1] Radiophysics Dept., Donetsk National University, 14 Hurova Av., Donetsk, 83001, Ukraine
[2] Electronic Eng. Dept, University of Rome Tor Vergata Via del Politecnico 1, 00133, Rome, Italy
Tel: +39 06 7259 7323; Fax. +39 06 7259 7935; E-mail: paolo.colantonio@uniroma2.it

***Abstract* - In this contribution, an inverse-class-*F* (*F*$^{-1}$) power amplifier at 1.7 GHz using GaN device is proposed and experimentally tested. The novelty in the design is the use of a three-layers rectangular slot resonators in microstrip line's ground plane as harmonic filter. In particular, a planar periodic structure composed by two different slot resonators is used to control 2nd, 3rd harmonics and to match to 50 Ω the fundamental frequency. Experimental results shows 60 % of drain efficiency and roughly 4 W of output power with 13 dB of associated gain.**

***Index Terms* - Class F, Inverse class F, Microstrip Slot, Power amplifiers.**

I. INTRODUCTION

The design of high efficiency power amplifier (PA) is usually based on a suitable waveform engineering in order to minimize the power dissipated in the active device and to increase the achievable output power at fundamental frequency [1]. In this context, several design solutions were deeply investigated, based on current- or switched-mode behavior of the adopted active device. In particular, the most simple and implemented solutions, based on the control of the output harmonic terminations only, are the class F and inverse class F [2,3]. Advantages of class *F* and *F*$^{-1}$ power amplifiers lie in the facts of high power utilize factor and straightforward strategy to design the output matching networks [2,3].

The load impedance seen at the drain of an ideal class F amplifier must ensure a half-sinusoidal shape of the drain current (the fundamental and even harmonics are present) and rectangular shape of the drain voltage (the fundamental and odd harmonics are present). In most practical cases, however, only the second and the third harmonic of the fundamental signal are tuned, neglecting the higher ones. This approach limits the maximum theoretically attainable efficiency of class F amplifier to 90% [2]. Conversely, the output matching network of a Class *F*$^{-1}$ has to ensure a short circuit condition at the third harmonic and an open circuit condition at the second one. In [5] simulation methods for both class *F* and *F*$^{-1}$ power amplifiers built on GaN transistors have been presented. Theoretical and experimental comparisons between the mentioned amplifier classes have also been presented in previous contributions [6-9].

In microwave frequency range, the PA's harmonic-filtering networks are traditionally implemented through a suitable combination of microstrip open/short circuit stubs [6,7]. In [10] a design method for class *F*$^{-1}$ by using a series of composite right/left handed (CRLH) transmission line (TL) and open CRLH-TL was presented. In this contribution, the design of a class *F*$^{-1}$ PA is done using microstrip slot resonators as output matching network [4]. In particular, a three-layer planar structure based on rectangular slot resonators in microstrip line's ground plane is used to control the level of harmonics. The approach is applied to design a power amplifier at 1.7 GHz using GaN commercial device. Experimental results showed 60 % of drain efficiency and roughly 4 W of output power with 13 dB of associated gain at 1.7 GHz.

II. AMPLIFIER DESIGN

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For the design of the Class F^{-1} amplifier, a commercial GaN device (Nitronex NPTB00004) is adopted. According to its data sheet, the following characteristics have been extracted:

- drain bias voltage, V_{ds} = 28 V;
- power gain, G= 15.5 dB;
- pinch-off voltage, V_p= -2 V;
- optimum source impedance, $Z_{s,opt@1.7\text{GHz}}$= 13.1 + j·24.3 Ω
- optimum load impedance, $Z_{L,opt@1.7\text{GHz}}$ = 34.5 + j·48.8 Ω

For the actual design, a class C bias condition (V_{gs}=–3V) has been adopted. According to the Class F^{-1} theory, the input and output optimum loads have been estimated using ideal tuners.

A. Output Matching Network Design

The output harmonic filter (FH) was realized by using a slot resonator in microstrip line ground plane, whose topology is shown in Fig.1.

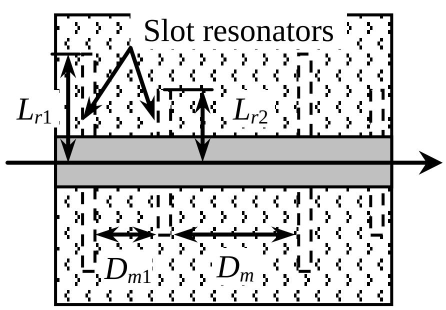

Fig.1 Designed harmonic filter.

The sizes of the two slot resonators L_{r1} and L_{r2} were calculated by transverse resonance method like rejection filters [11,], in order to meet the required harmonic loads at the second and the third harmonics of 1.7 GHz. Instead, the generalized scattering matrix of the finite size periodic structure was calculated in AWR environment to account for the effect of mutual coupling between the slot resonators [12].

The structure performs filtration of the output signal's harmonics in the frequency range 2.6–5.2 GHz. Such a filter and its simulated behavior were subsequently used in the design of the power amplifier to design the complete output network, i.e. to fulfill the power matching condition for the fundamental frequency [13]. Its scattering matrix was calculated separately and then included into amplifier schematic.

The resulting complete schematic of the output matching network is shown in Fig.2, which include, among others, the parasitic of the transistor's package (lumped elements), the microstrip line stubs and the FH built on narrow rectangular slot resonators.

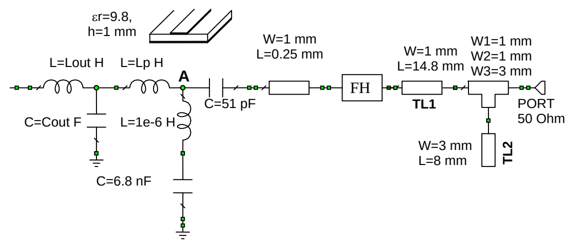

Fig.2 Output matching network of class F^{-1} PA.

The tuning of the amplifier was performed according to the following procedure. By varying the parameters D_{m1} and D_m the FH was tuned for transmission of the signal at fundamental frequency and reflection of second and third harmonics with phase difference between them equal to π [8]. Then, by varying the lengths of the microstrip line sections D_m and TL1, and the length of the open stub TL2, the scheme was tuned to maximize output power and efficiency at the operating frequency f_0=1.7 GHz. The input impedance of the optimised output matching network without parasitic elements (L_{out}, C_{out} and L_p) is shown in Fig.3. In the same figure are also reported the ideal values of the fundamental, second and third harmonics loads estimated by ideal tuners.

The simulated intrinsic voltage V_{ds} and current I_d output waveforms of the transistor are shown in Fig. 4. This gives the following values of the impedance $Z(nf_0)=V_{ds}(nf_0)/I_d(nf_0)$ at the fundamental frequency and higher harmonics:

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$Z(f_0)=46\cdot e^{-j136°}\,\Omega$; $Z(2f_0)=34\cdot e^{+j90°}\,\Omega$; $Z(3f_0)=49\cdot e^{-j95°}\,\Omega$.

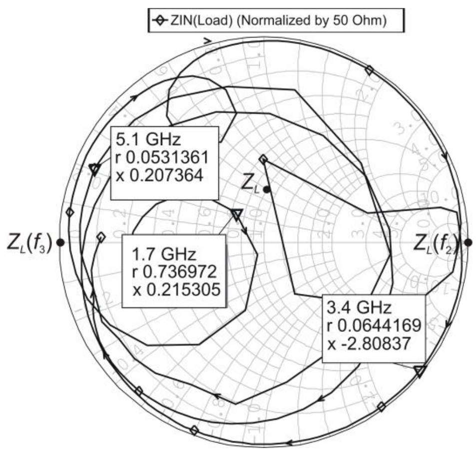

Fig.3 Frequency behavior of the input impedance of the output matching network.

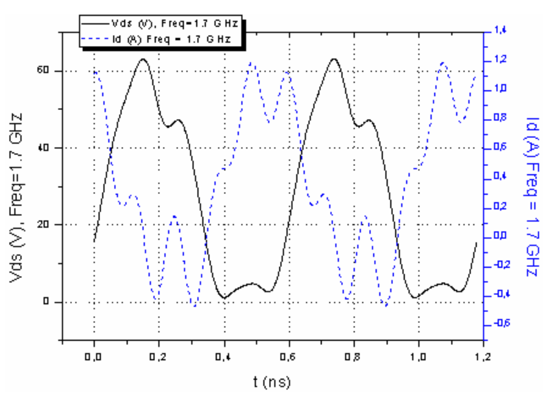

Fig 4 Simulated intrinsic waveforms of the GaN transistor at 1.7 GHz with drain and gate bias voltages of 28 V and –3.0 V, respectively.

B. Input Matching Network Design

The input matching network of the amplifier was designed to convey maximum power to the transistor gate. Referring to Fig.5(a), the network consists of feed transmission line (section TL3) with 50 Ω characteristic impedance, and capacitive open stub TL4. The tuning of the input network was done by varying the lengths of these stubs. The value of the impedance presented to the transistor gate (port 2 of schematic in Fig.5(a) is ZS=11.5+j·20.5 at the operating frequency, corresponding to the conjugate input impedance of the device. In Fig. 5(b) is reported the simulated behavior of such impedance.

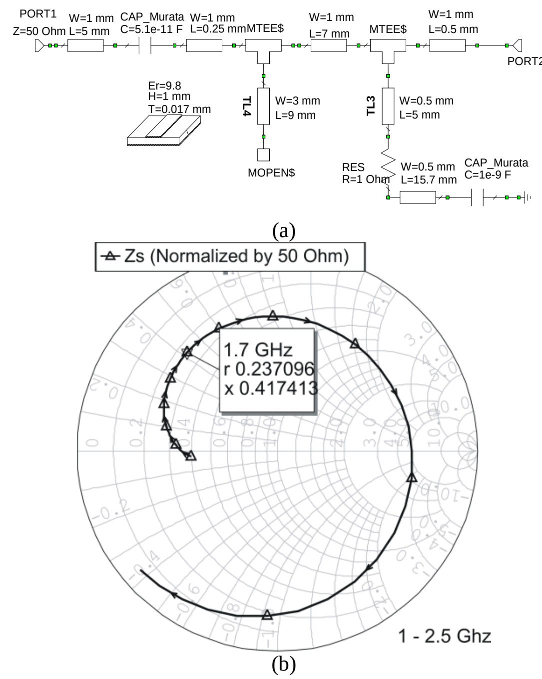

Fig.5 (a) Electric scheme and (b) source impedance of PA input matching network.

C. Complete Prototype

The printed circuit board for the FH and the whole amplifier is manufactured on polymer material with thickness h=1.0 mm and dielectric constant ε_r=9.8.

The final topology of the PCB is shown in Fig.6. The PCB is placed in the enclosure shield and its lower part is used for the slot resonators activity.

Photography of the realized Class F^{-1} PA is shown in Fig. 7. In the PA implementation the harmonic filter built on slot resonators is confined in a volume of 30×38 mm^2 surface with 7 mm depth.

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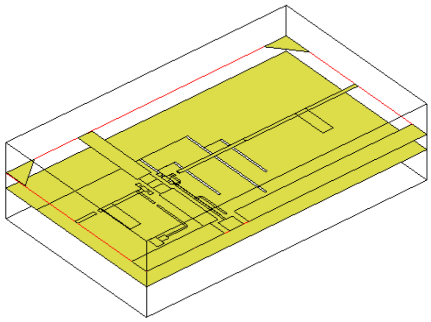

Fig.6 Class F^{-1} power amplifier topology.

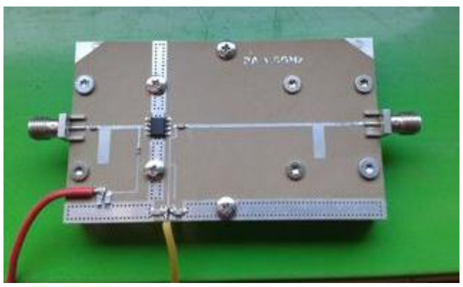

Fig.7 Photo of the realized class-F^{-1} power amplifier.

III. EXPERIMENTAL RESULTS

The realized amplifier was measured in continuous wave (CW) condition. In Fig. 8 are reported the measured output power and power added efficiency at 1.7 GHz versus the input power. A saturated output power of 35dBm was measured (2dB lower than simulated) with 60% of PAE.

Similarly, in Fig. 9 are reported the frequency behaviors of output power and power added efficiency, measured for a constant input power P_{in}=22.4 dBm (i.e., corresponding to the saturation condition from Fig. 8). Also in this case a slight difference between simulations and measurements were observed for the output power. Such a difference, after a reverse engineering, was ascribed to the device commercial model, typically optimized for a class-B or AB operation [14]. This implies that the model accuracy may be compromised in the high-efficiency load-line region and by class C biasing point.

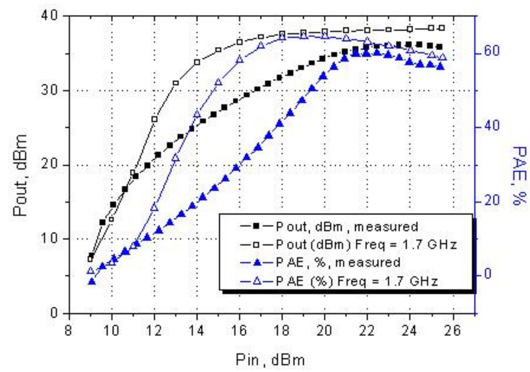

Fig. 8. Simulated (empty symbols) and measured (filled symbols) output power and power-added efficiency versus input power at 1.7 GHz. Drain and gate bias voltages are 28V and –3.0V, respectively.

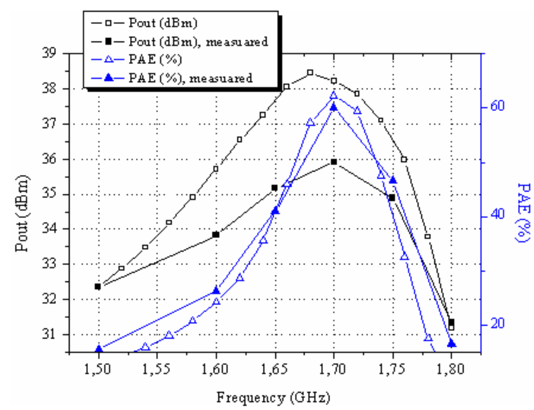

Fig. 9 Simulated (empty symbols) and experimental measured (filled symbols) performances.

IV. CONCLUSIONS

In this contribution, a class F^{-1} power amplifier built on NPTB00004 GaN transistor, with manipulation of higher harmonics of output signal based on slot resonator structure was simulated, designed and experimentally investigated. Filtering of the second and third harmonics of fundamental signal accompanied by tuning of the phase difference between them was performed using slot resonators in microstrip line's ground plane. Efficiency of the power

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amplifier at the frequency of 1.7 GHz was 60 % at the output power of 3.9 W.

REFERENCES

[1] P. Colantonio, F. Giannini, and E. Limiti, *High Efficiency RF and Microwave Solid State Power Amplifiers*. Hoboken, NJ: Wiley, 2009.

[2] F. H. Raab, "Class-F power amplifiers with maximally flat waveforms," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 2007–2012, Nov. 1997.

[3] F. H. Raab, "Maximum efficiency and output of class-F power amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. 49, no. 6, pp. 1162–1166, June 2001.

[4] Rassokhina Yu. V., Krizhanovski V.G. Periodic Structure on the Slot Resonators in Microstrip Transmission Line // IEEE Transactions on Microwave Theory and Techniques. - Vol. 57, No. 7. – July 2009. – P. 1694-1699.

[5] J. H. Kim, G. Do Jo, J. H. Oh at al. "Modeling and Design Methodology of High-Efficiency Class-F and Class-F^{-1} Power Amplifiers," *IEEE Trans. Microwave Theory Tech*., vol. 59, no. 1, pp. 153-165, Jan. 2011.

[6] Y. Y. Woo, Y. Yang, and B. Kim, "Analysis and experiments for high-efficiency class-F and inverse class-F power amplifiers," *IEEE Trans. Microwave Theory Tech.***,** vol. 54, no. 5, pp. 1969–1974**,** May 2006**.**

[7] Y. Y. Woo, Y. Yang, I. Kim, and B. Kim, "Efficiency comparison between highly efficient class-F and inverse class-F power amplifiers," *IEEE Microwave Mag.***,** vol. 8, no. 3, pp. 100–110**,** June 2007**.**

[8] E. Cipriani, P. Colantonio, F. Giannini, R. Giofrè, "Theoretical and Experimental Comparisons of Class F vs. Class F-1 PAs," *Proceedings of the European Microwave Conference*, EUMC 2010, Paris, France, Sept. 2010, pp. 1670-1673.

[9] V. Carrubba, A. L. Clarke, M. Akmal, J. Lees, J. Benedikt, P. J. Tasker, S. C. Cripps, "On the Extension of the Continuous Class-F Mode Power Amplifier", *IEEE Trans. Microwave Theory Tech.***,** vol. 59, no. 5, pp. 1294–1303**,** May 2011**.**

[10] Dupuy A. Inverse Class-F Power Amplifier Using Composite Right/Left-Handed Transmission Lines as a Harmonic Trap / A. Dupuy, K. M.K.H. Leong, R. Staraj, G. Jacquemod, T. Itoh // *Proceedings of the 36th European Microwave Conference* – 2006. 10-15 Sept, Manchester – P. 360-363.

[11] Kryzhanovskiy V.G., Rassokhina Yu.V. The transverse resonance technique modification for analysis of slot resonators in microstrip line ground plane // *Microwave and Telecommunication Technology (CriMiCo), 2011, 21th International Crimean Conference 12-16 Sept. 2011. Conference Publications*. – vol. 2 – pp. 601–602.

[12] Yu. V. Rassokhina, V. G. Krizhanovski, "Analysis of coupled slot resonators of complex shape in metalization plane of a microstrip transmission line using the transversal resonance techniques," *Radioelectronics and Communications Systems*, vol. 55, No 5, pp. 214-222, May 2012 (ISSN 0735-2727).

[13] Kryzhanovski, V.G., Rassokhina, Yu.V., Colantonio, P. The output circuit of inverse class F power amplifier with slot resonators in the microstrip line ground plane // *Microwave and Telecommunication Technology (CriMiCo), 2011, 21th International Crimean Conference 12-16 Sept. 2011. Conference Publications*. – vol. 1 – pp. 141–142.

[14] H. M. Nemati, P. Saad, Ch. Fager, and K. Andersson, "High-Efficiency Power Amplifier," *IEEE Microwave Magazine*, vol. 12, no. 1, pp. 81–84**,** Feb**.** 2011**.**