Enhancement in Performance of sub-100nm MOSFETs With Gate Stack Architecture

Tina Mangla¹, Amit Sehgal²,#, Mridula Gupta¹, R. S. Gupta¹,*

¹ Semiconductor Device Research Laboratory, Department of Electronic Science, University of Delhi South Campus, New Delhi – 110021, INDIA
e-mail: tinamangla@yahoo.com; rsgu@bol.net.in*
² Department of Physics and Electronics, Hansraj College, University of Delhi, New Delhi - 110007, INDIA
# e-mail: amitsehgal112@yahoo.com

Abstract - A 2-D analysis for different gate stack dielectric structured MOSFETs with carrier quantization effects is presented using Green’s function for solving Poisson’s equation. Explicit results for potential distribution, threshold voltage and drain current are presented. Based on extensive simulation and developed formulation, it is found that using double-layer gate stack structures with low-k dielectric as spacer material can well confine the electric fields within the channel. Comparison of the results thus obtained is done with simulated results to justify the analysis.

Index Terms - Gate stack, Quantum effects, MOSFET, Device modeling.

I. INTRODUCTION

The current trend in scaling down of silicon metal-oxide-semiconductor field-effect-transistor (MOSFET) feature size has led to the fabrication of devices in which channel length approach deep submicron dimensions. As dictated by scaling rules, the decrease in channel length must be accompanied by an increase in the channel doping density and a decrease in the gate-oxide thickness [1]. These two effects together, make the potential well for the inversion layer carriers very narrow and steep. As a result, the energies of the inversion layer carriers are quantized in the direction normal to the interface between the semiconductor and the oxide. Quantum mechanical (QM) effects in MOSFET inversion layers have been studied for long [2-4] and it is by now widely accepted that quantum effects must be taken into account for the qualitative description of sub 100nm MOSFETs’ device characteristics [4-8]. Therefore, analytical models for them need to be established for circuit designers. In [5], an analytical QM model is developed. However, only the 1-D effects were taken into account. But, when the gate becomes so short, that the gate length is comparable to the channel depth; a need of 2-D analytical model accounting for QM effects in MOSFETs arises. In terms of numerical and device simulations, there have been extensive works on 2-D QM effects, but the self-consistent solutions obtained by coupling Schrödinger’s equation to Poisson’s equation involves sophisticated numerical iterative methods, and device simulation results obtained don’t describe analytical relationship between the geometry structure and its electrical behavior. Another modeling issue is about the introduction of high-k gate or gate-stack architecture (multiple material layers) in sub 100 nm MOSFETs, which have drawn great concern [5, 9].

In this context, an analysis comprising of 2-D effects together with the effect due to different dielectric configurations and quantized carrier density has been carried out in this paper. The framework comprises of solving 2-D Poisson’s equation using Green’s function, while Schrödinger’s equation is decoupled using triangular potential well (TPW) approximation, to obtain potential distribution formulation with the above said effects.
II. MODELING AND DISCUSSION

A. Poisson’s equation and quantum effects

Fig.1 shows the cross-sectional view of n-channel MOSFET together with different gate dielectric configurations studied: (i) conventional $SiO_2$ as gate dielectric; (ii) high-$k$ dielectric with same physical thickness as of device i; (iii) two layer stacked-gate dielectric configuration of high-$k$ and $SiO_2$ (high-$k$-$SiO_2$-$Si$) with same physical thickness as of device i; (iv) two layer stack-gate dielectric configuration of $SiO_2$ and high-$k$ ($SiO_2$-high-$k$-$Si$) with same physical thickness as of device i; The figure also shows rounded source/drain ohmic contacts and the formulation incorporates the rounded source/drain contact effect i.e. junction curvature effect. The device under consideration has been divided into three regions: region I (gate-dielectric), region II (sandwiched dielectric or spacer layer) and region III (silicon substrate).

The Poisson equation for the same is given as:

$$
\nabla^2 \Phi(x, y) = \begin{cases} 
0 & 0 \leq y \leq -t_{k2} \\
-t_{k1} + t_{k2} & -t_{k2} \leq y \leq 0 \\
-\frac{\rho(x, y)}{k_{Si}} & 0 \leq y \leq Y_{DD} 
\end{cases}
$$

(1)

where $t_{k1}(t_{k2})$ is the physical thickness of gate dielectric with dielectric permittivity $k_{j}(k_{Si})$, $k_{Si}$ is the dielectric permittivity of silicon substrate (region III), $k_{SiO_2}$ is the dielectric permittivity of $SiO_2$ ($k = 3.9$) and $Y_{DD} = \sqrt{(y_j + Y_{dd})^2 - y_j^2}$, where $y_j$ is the junction depth, and $Y_{dd}$ is the drain-end depletion width. $\rho(x, y)$ is the 2-D space charge density distribution in the silicon substrate given as:

$$
\rho(x, y) = \begin{cases} 
-q \left( N_A + \frac{N_{inv}}{Y_{inv}} \right) & 0 \leq y \leq Y_{inv} \\
-q \cdot N_A & Y_{inv} \leq y \leq Y_{d0} \\
0 & Y_{d0} \leq y \leq Y_{DD} 
\end{cases}
$$

(2)

Here, $N_A$ is the substrate doping density, $L$ is the channel length and $Y_{d0}$ is the one-dimensional (1-D) depletion width. The $N_{inv}$, inversion space charge density and inversion layer width $Y_{inv}$, are expressed accordingly [5] by solving Schrödinger’s equation under (TPW) approximation [2].

B. Potential distribution modeling

To estimate the potential solution over the 2-D space (along the device length and device depth), the Green’s theorem [10] is applied and the potential solution is given as:

$$
\Phi(x, y) = \int \int \frac{\rho(x', y')}{\varepsilon} \cdot G(x, y; x', y') dx' dy' + \int_s \frac{\partial \Phi(x', y')}{\partial n'} \cdot G(x, y; x', y') dS \\
- \int_s \Phi(x', y') \cdot \frac{\partial G(x, y; x', y')}{\partial n'} dS'
$$

(3)
where \( G(x, y; x', y') \) is Green’s function solution and \( \rho(x', y') \) contributes the space charge density with carrier quantization effects.

Table I: The List of Boundary Conditions used in the analysis for different regions

<table>
<thead>
<tr>
<th>Region</th>
<th>Boundary Condition</th>
</tr>
</thead>
</table>
| I      | \[
V_{eff} = V_{gs} - V_p \quad y = -(t_{i1} + t_{i2}) \\
V_0 + \frac{t_{i1}}{t_{i2}} (y + t_{i2}) \quad x = 0 \\
V_i + \frac{t_{i2}}{t_{i1}} (y + t_{i2}) \quad x = L \\
D^I(x, y) = k_i E^I_y(x, y) \quad y = -t_{i2}
\] |
| II     | \[
\begin{align*}
& D^I(x, y) = k_i E^I_y(x, y) \quad y = -t_{i2} \\
& V_{bi} + V_0 - V_{eff} \quad x = 0 \\
& V_i + V_{bi} + V_{ds} - V_L \quad x = L \\
& D^I(x, 0) = k_i E^I_y(x, 0) \quad y = 0
\end{align*}
\] |
| III    | \[
\begin{align*}
& D^I(x, 0) = k_i E^I_y(x, 0) \quad y = 0 \\
& V_i \left(1 - \frac{y}{Y_{SD}}\right)^2 \quad x = 0 \cap y \leq Y_{SD} \\
& V_i \left(1 - \frac{y}{Y_{SD}}\right)^2 \quad x = 0 \cap y > Y_{SD} \\
& (V_{bi} + V_{ds}) \left(1 - \frac{y}{Y_{DD}}\right)^2 \quad x = L \cap y \leq Y_{DD} \\
& 0 \quad y = Y_{DD}
\end{align*}
\] |

where \( V_0 = V_{gs} - V_{eff} \) and \( V_L = V_{bi} + V_{ds} - V_{eff} \).

A distinct feature of the solution developed is that, it depends upon the boundary conditions chosen and the space charge density in the region, and itself includes short channel effects (SCEs) and drain induced barrier lowering (DIBL) effect. In comparison with simulation technique, our analysis solves fewer equations and in particular have freedom of variable change when calculation of a value over a position is required, rather than solving the whole device system.

The reduced formulation of potential solution for region of concern i.e. silicon substrate is obtained by using (3), and applying boundary conditions listed in Table 1 is expressed as:

\[
\Phi^Si(x, y) = \int \frac{\rho(x', y')}{k_S^i} G(x, y; x', y') dx' dy' + \sum_m \frac{D^m}{k_S^i} \sin(c_m(Y_{DD} - y)) \sin(c_m x) \\
\times \left[ P_n^{Sin} \sinh(c_m^m (L - x)) \right] + \sum_n \sin(c_n^m L)
\]

where \( \Phi^Si(x, y) \) is the potential solution of silicon substrate, \( Y_{sd}/Y_{dd} \) is the source/drain end depletion width; \( c_n^i = (n - 0.5)\pi/t_{i1} \), \( c_n^ii = n \cdot \pi/t_{i2} \), \( c_n^iii = (n - 0.5)\pi/Y_{DD} \) is the eigenvalue along \( y \)-direction for \( i \)th region (i=I, II, III), and \( c_m^i = m\pi/L \) is the eigenvalue along \( x \)-direction. \( P_n^i(P_n^{di}) \) are the Fourier coefficients of potential distribution in region \( i \) (i=I, II, III) and \( D_m^i \) is the electric field displacement. The Fourier coefficients \( P_n^i(P_n^{di}) \) for different regions and \( D_m^i \) which refers to the unknown boundary condition Fourier coefficient at \( y=0 \) i.e. at spacer dielectric/Si interface are expressed in Appendix. \( V_{bi} \) is the built-in voltage, \( Y_{SD} = \sqrt{(y_j + Y_{sd})^2 - y_j^2} \) where \( Y_{sd} \) is the source-end depletion width, \( V_{eff} \) is the effective gate voltage (listed in Table 1), \( V_{gs} \) is the gate-source voltage, \( V_{ds} \) is the drain-source voltage, \( V_{fb} \) is the flat band voltage, \( V_0 \) and \( V_L \) are listed in Table I. Thus the complete potential solution for silicon substrate \( \Phi^Si(x, y) \) is given by employing \( D_m^i \) and other potential Fourier coefficients in (4). All calculations were made for temperature \( T=300K \), \( W=50nm \), \( L=50nm \),
y_i = 10nm, \( N_A = 5 \times 10^{24} \) m\(^3\), \( V_{ds} = 0.01V \) and \( t_{d1} + t_{d2} = 3nm \).

![Fig. 2 Variation of surface channel potential with normalized channel distance for devices shown in Fig. 1. \( (V_{gs} = 0.1V) \)]

Surface channel potential variation with normalized channel distance \((x/L)\) has been plotted in Fig. 2 for different gate dielectric combinations explained in Fig. 1. While comparing curves of device i and device ii in Fig. 2, it is seen that with the increase in gate dielectric constant, a drastic increase in the overall channel potential occurs. This is due to the fact that increase in dielectric constant increases the capacitance of gate dielectric for the same physical thickness. This increased capacitance increases the electric field acting at dielectric/Si interface and thus depletes more charges in the silicon substrate, thereby increasing the surface channel potential. On analyzing the curves of devices iii and iv, it is observed that the arrangement of gate stack structure influences difference in the scheme of curves. This is because of the different behavior of electric field lines while switching from one medium to another. Thus, the effective field lines acting on silicon substrate are not the same in device iii and iv.

C. Transfer characteristics and threshold voltage modeling

1) Sub-threshold current

For long device dimensions, the surface potential distribution is flat over a range along the channel in the sub-threshold regime. But, switching to small device dimensions deviates this flat behavior and methodology of choosing minimum surface potential is required to be adopted to evaluate drain current characteristics in sub-threshold regime. The current in this region is dominated by diffusion component of current [11] and is given as:

\[
I_{ds} = \mu_n \cdot \frac{W}{L} \cdot \left( \frac{q \cdot k_{Si} \cdot N_A}{2 \cdot \phi_{x=0} \cdot \sqrt{N_A}} \right) \cdot \left( \frac{V_t \cdot n_i}{N_A} \right)^2 \cdot \exp\left( \frac{\phi_{x=0} - V_t}{V_t} \right) \cdot \left( 1 - \exp\left( -\frac{V_{ds}}{V_t} \right) \right)
\]

where \( \mu_n \) is the doping dependent low-field mobility, \( V_t \) is the thermal voltage, \( n_i \) is the intrinsic carrier concentration, \( W \) is the channel width, and the minimum surface potential \( \phi_{x=0} = \Phi_{Si}(x_{min, 0}) \) is evaluated by setting the derivative of \( \Phi_{Si}(x, y) \) along \( x \)-direction equal to zero to obtain point of minima i.e. \( x = x_{min} \).

2) Threshold Voltage

In this work, \( V_{th} \) modeling is based on the solution of 2-D Poisson’s equation, with quantized carrier density incorporated in space-charge density. In our analysis, diffusion current equation (5) using the current criterion \( I_{ds} = I_{th} = 10^{-8} \times (W/L) \) Amperes is used to extract the threshold voltage of the device, which in-turn relates to an extrinsic measurable quantity from experimental overview.

The variation of threshold voltage with channel length for device i and device ii with different dielectrics is shown in Fig. 3. The modeled results
are found to be in good agreement with simulated results [12]. The scaling down of channel length shows roll-off in the threshold voltage values, which proves the incorporation of short channel effect, introduced at small device dimensions. This can be explained as; when channel length decreases, the effective area to be depleted reduces, and this reduced area is depleted at lower gate voltage or a lower value of threshold voltage is realized. With increase in dielectric constant of gate dielectric at constant physical thickness for a given channel length, a rapid decrease in threshold voltage can be seen. This is due to the fact that increase in dielectric constant increases the dipole action, which influences rapid depletion of charges and thus early onset of inversion of carriers occurs. This early inversion can be realized as decrease in the applied gate voltage to obtain a given depletion and thus decreasing the device threshold voltage.

![Threshold voltage variation with channel length.](image1)

The error in threshold value in device iii and iv and threshold voltage variation for device iii with channel length is plotted in Fig.4 and its inset respectively. The modeled results are in good agreement with simulated results [12]. On comparing Fig.3 (for device i and ii) and Fig.4 (for device iii and iv), it can be inferred that $V_{th}$ of device iii and iv lies in between $V_{th}$ of device i and ii. This is because device iii and iv gate stack structure is a combination structure of device i and device ii dielectric constants; and thus have equivalent oxide thickness in between their equivalent oxide thicknesses. Previous studies suggest that, device iii and iv should predict the similar threshold voltage characteristics by equivalent oxide thickness concept, and would not be affected by positioning of dielectric layer. But, it can be seen from the Fig.4 that the difference in the threshold voltage arises. Although the difference decreases with increase in channel length, but at shorter channel length threshold voltage roll-off and error in threshold voltage rises. Further, switching from high-$k=10$ to 20, even though a decrease in $V_{th}$ occurs, but the difference of $V_{th}$ increases. Thus, the difference becomes more significant below 100nm channel length and switching to high-$k$ dielectrics, and shows incompetence of approximating both devices (device iii and device iv) to behave identically. Another inference drawn from the curves is that the threshold value for device iv is more as compared to device iii; as

![Difference in Threshold voltage with channel length.](image2)
when high-\( k \) layer is kept in contact with silicon substrate, the field lines diverge more (field lines diverge when entering from denser to rarer medium) and gate loses its control over the channel. Whereas, when the \( SiO_2 \) layer is in contact with substrate, the control of field lines is more focused on the channel. Thus, it is advised to use a low-\( k \) gate dielectric (\( SiO_2 \)) as spacer layer, to well confine the electric fields within the channel region and thus yield low \( V_{th} \) values for low power consumption.

3) ON-State Current

The linear region drain current [11] is given by:

\[
I_{ds} = -\mu_n \cdot W \cdot Q_{inv} \cdot \frac{E_x}{1 + \left(\frac{\mu_n}{v_{sat}}\right) \cdot E_x}
\]

(6)

where \( E_x \) is the horizontal electric field along the channel length, \( v_{sat} \) is the carrier velocity and \( Q_{inv} \) is the inversion charge density given by:

\[
Q_{inv} = -C_k \cdot \left(V_{gs} - V_{th} - \lambda \cdot V_{ds}\right)
\]

(7)

in which \( C_k \) \((C_k = [t_{k1}/k_1] + [t_{k2}/k_2])^{-1}\) is the gate dielectric capacitance per unit area and \( \lambda = (1 + f_L \cdot \delta) \) is the short channel coefficient [11]. Substituting (7) in (6) and integrating w.r.t. \( x \) from 0 to \( L \), we get

\[
I_{ds} = \frac{W \cdot \mu_n \cdot C_k}{L + \frac{\mu_n \cdot V_{ds}}{v_{sat}}} \left(V_{gs} - V_{th}\right) \cdot V_{ds} - \lambda \cdot \frac{V_{ds}^2}{2}
\]

(8)

To evaluate saturation drain current, saturation drain-source voltage (\( V_{dsat} \)) is evaluated using pinchoff condition

\[
\frac{\partial I_{ds}}{\partial V_{ds}} \bigg|_{V_{ds} = V_{dsat}} = 0
\]

(9)

And thus the same drain current equation (8) is extended to evaluate saturation drain current by replacing \( V_{ds} \) with \( V_{dsat} \). In the saturation regime, a prominent effect known as channel length modulation (CLM) is seen, and can be realized as shortening of effective channel length from \( L \) to \( L - L_{CLM} \), where

\[
L_{CLM} = \sqrt{\frac{2 \cdot k_{Si} \cdot (V_{ds} - V_{dsat})}{q \cdot N_A}}
\]

(10)

Thus, drain current in the saturation region is expressed by replacing \( L \) by \( L - L_{CLM} \) and \( V_{ds} \) by \( V_{dsat} \) in (8).

Fig.5. Drain Current variation with gate voltage for devices shown in Fig.1

Drain current variation with gate voltage for different dielectric combination MOSFETs demonstrated in Fig.1, is shown in Fig.5. The modeled results match fairly well with simulated results [12]. It can be seen from the figure, that a rise in dielectric constant enhances the drain current performance as an increase in dielectric constant decreases the threshold voltage and thus increases the inversion carrier concentration at same gate voltage. This increased carrier density flow is accounted as an increase in drain current flow of the device. While, the comparison amongst device iii and device iv characteristics shows an improvement in drain characteristics of device iii. This can be explained from Fig.4, in which the device iii threshold voltage is found to
be less as compared to device iv for same dielectric thicknesses and constants. The high current performance of device iii configuration proves to be a merit over device i and by suitably altering the high-\(k\) dielectric thickness of device iii, the requirement of reducing the gate tunneling transport phenomena together with high drive current can be achieved.

III. CONCLUSION

The two-dimensional analysis of gate stack sub-100nm MOSFETs including quantization effects have been done. The work aims at solving 2-D Poisson equation with quantization effects incorporated as TPW approximation in space charge density. The results obtained are found to be in good agreement with simulated results. In the work, various gate stack structures were examined. The choice of low-\(k\) dielectric spacers in double-layer gate stack MOSFETs is found to be device of merit because of low \(V_{th}\) value and high drive current as compared to device i and iv. Or, in other words, better gate controllability over the channel can be achieved from a structure with a double-layer gate stack having low-\(k\) dielectric spacers as compared to high-\(k\) dielectric spacers.

APPENDIX

The Fourier coefficients, \(P_n^{Si}(P_n^{Di})\) of potential distribution in region \(i\)

\[
P_n^{Si} = \frac{2}{t_{k2}} \int_{-t_{k2}}^{0} \varphi'(0, y') \cos(c_n^{i'} y') dy' \quad (A1)
\]

\[
P_n^{Di} = \frac{2}{t_{k1}} \int_{-t_{k1}}^{0} \varphi'(L, y') \cos(c_n^{i'} y') dy' \quad (A2)
\]

\[
P_n^{SIII} = \frac{2}{Y_{DD}} \int_{0}^{y_p} \varphi''(0, y') \cos(c_n^{i'} y') dy' \quad (A3)
\]

\[
P_n^{SIII} = \frac{2}{Y_{DD}} \int_{0}^{y_p} \varphi''(0, y') \cos(c_n^{i'} y') dy' \quad (A4)
\]

\[
P_0^{SIII} = \frac{1}{t_{k2}} \int_{-t_{k2}}^{0} \varphi''(0, y') dy' \quad (A5)
\]

\[
P_0^{SIII} = \frac{1}{t_{k2}} \int_{-t_{k2}}^{0} \varphi''(0, y') dy' \quad (A6)
\]

\[
P_n^{SIII} = \frac{2}{Y_{DD}} \int_{0}^{y_p} \varphi''(0, y') \cos(c_n^{i'} y') dy' \quad (A7)
\]

\[
P_n^{SIII} = \frac{2}{Y_{DD}} \int_{0}^{y_p} \varphi''(L, y') \cos(c_n^{i'} y') dy' \quad (A8)
\]

\[
D_m^{Si} \text{, the electric field displacement can be obtained using following set of equations:}
\]

\[
\alpha(m) = \frac{2(1 - (-1)^n)}{m \pi} \frac{V_{eff} \cdot L}{2 \cosh(c_m t_{k1})} \quad (A9)
\]

\[
\beta_n(m) = \left( P_n^{Si} + (-1)^{n+1} P_n^{Di} \right) \frac{k_m}{c_m^2 + (c_n^{i'})^2} \quad (A10)
\]

\[
\xi(m) = \frac{\left( P_n^{SIII} + (-1)^{n+1} P_n^{SIII} \right)}{c_m} \quad (A11)
\]

\[
\gamma_1(m, k, T) = \frac{L}{2 \cdot k \cdot c_m} \frac{\sinh(c_m T)}{\cosh(c_m T)} \quad (A12)
\]

\[
\gamma_2(m, k, T) = \frac{L}{2 \cdot k \cdot c_m} \frac{\cosh(c_m T)}{\sinh(c_m T)} \quad (A13)
\]

\[
\gamma_3(m, k, T) = \frac{L}{2 \cdot k \cdot c_m} \frac{1}{\sinh(c_m T)} \quad (A14)
\]

\[
\kappa(m) = \int \left[ \int_{V} \frac{\rho(x', y')}{k_S} \cdot G^{III}(x, y', y') dx' dy' \right]_{y=0} \times \sin(c_m x) dx
\]

\[
\kappa(m) = \int \left[ \int_{V} \frac{\rho(x', y')}{k_S} \cdot G^{III}(x, y', y') dx' dy' \right]_{y=0} \times \sin(c_m x) dx
\]
\[
D_i(m) = \left[ \alpha(m) - \xi(m) + \sum_n \beta_n^i(m) + (-1)^{n+1} \beta_n^II(m) \right] \gamma_1(m, k_2, t_{k2})
\]

(A16)

\[
D_2(m) = \left[ \kappa(m) - \xi(m) + \sum_n \beta_n^{III}(m) - \beta_n^{II}(m) \right] \left\{ \gamma_1(m, k_1, t_{k1}) + \gamma_2(m, k_2, t_{k2}) \right\}
\]

(A17)

\[
\gamma_R(m, k_1, k_2, k_{Si}, t_{k1}, t_{k2}, Y_{DD}) = \left\{ \gamma_1(m, k_1, t_{k1}) + \gamma_2(m, k_2, t_{k2}) \right\}
\times \left\{ \gamma_3(m, k_2, t_{k2}) + \gamma_1(m, k_{Si}, Y_{DD}) \right\}
\]

(A18)

\[
D_m^{si} = \frac{D_1(m) - D_2(m)}{\gamma_R(m, k_1, k_2, k_{Si}, t_{k1}, t_{k2}, Y_{DD}) - \{\gamma_3(m, k_2, t_{k2})\}^2}
\]

(A19)

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