Trends in High-Efficiency Power Amplifier Design Solutions

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Abstract - In this contribution, research activities and trends in the field of RF and microwave power amplifiers design are discussed. Strategies for high efficiency are focused and the results attained presented, showing state-of-the-art power amplifier design, utilising GaAs or GaN technologies. Some “evergreen” design solutions, recently rediscovered for advanced communication systems, as the Doherty and Envelope Tracking approaches, are revisited.

Index terms: Power Amplifiers, High Efficiency, Amplifier Linearity, Device Technologies, Doherty, Envelope Tracking.

I. INTRODUCTION

The power amplifier (PA) is a key element in transmitter systems, whose main task is to increase the power level of signals at its input up to a predefined level. PA’s features are mainly related to the absolute output power levels achievable, accompanied to highest efficiency and linearity performances. In fact, regardless from the specific application considered, from the energetic point of view a PA acts as a component converting dc power from supplies ($P_{dc}$) into microwave power ($P_{out}$). Therefore it is clear that highest efficiency levels become mandatory to reduce dc power consumption. On the other hand, a linear behaviour is clearly mandatory to avoid the corruption of the transmitted signal information. Unfortunately, efficiency and linearity are contrasting requirements, forcing the designer to a suitable trade-off. Moreover, as contrasted to low-level amplifiers, often specified in term of small-signal gain, the requirement of highest output power levels implies the selection of the active devices composing the PA and the exploration of their non-linear operating regions, to fully exploit the output power capabilities [1]. Since PAs are employed in a broad range of fields, the large differences in system applications are typically reflected back into the technologies adopted for PAs active modules realisation [2]. However, from the designer perspective, a PA is a non-linear system component, thus requiring dedicated non linear design methodologies to attain the highest available performance [1].

In this contribution, starting from an overview of the available technologies for PA realisation and related performances, the PA design strategies for high efficiency and high linearity performances are revisited and established through several experimental results carried out. Some “evergreen” design solutions, as the Doherty and Envelope Tracking approaches, recently re-discovered for advanced communication systems, are revisited trying to identify their strength and potentials. Finally, due to the increasing demand of PAs for multi-band and/or multi-standard applications, suitable design solutions are discussed, indicating a possible research roadmap and trends.

II. TECHNOLOGIES FOR SOLID STATE PAS

In the last decade, the rapid improvement of mobile and personal communications systems, ranging from cellular telephony to wireless LAN, with the corresponding request of high quality radio links, is posing a major challenge to high frequency technologies and subsystem performance, above all in the microwave frequency region. Moreover, the recent trends toward higher and higher power densities, mainly pushed by radar and electronic warfare applications, is the latest development of the tremendous advancements experienced by the high-frequency semiconductor industry. While in
the upper microwave and lower millimetre wave range many efforts have been devoted towards the development of active devices with high power densities, a minor progress has been experienced in the lower GHz range. For the former, for instance, the development of “field plate” gate extensions over the drain region applied to GaAs or GaN FET structures, resulting in a breakdown voltage increase, is pushing such technology to become a serious competitor of LDMOS in L- or S-Band applications [3]. Simultaneously, production of GaN HFET devices has been initiated, to further increase device power densities thanks to the highest breakdown voltages assured from such wide bandgap material [4]. Even if the lack of technological maturity is still a drawback for GaN technology, a rapid improvement of manufacturability and yield can be forecasted, with the goal of developing high power solid state PAs, eventually replacing present TWT and solid-state amplifiers in all base-stations applications. On the contrary, the minor progress in output power experienced at lower frequencies, is mainly due to different system requirements: in this case major emphasis is devoted to linearity performances (due to complex modulation schemes) rather than on absolute output power levels. The major RF power technologies are reported in Fig. 1, as related to the relevant applications with the corresponding output power.

III. DESIGN APPROACHES

PA design is strongly dependent on operating frequency and application requirements, as well as to the available device technology: this situation often results in an exciting challenge for PA designers, since available approaches are not unique. Moreover, the design is further complicated by the non linear active device behaviour, even if simplified approaches are often employed to infer preliminary device figures [5]. The developed PA is therefore often the result of a trade-off between conflicting requirements, as linearity vs. efficiency or high output power vs. low distortion. For high frequency applications however it is possible to identify two broad classes of PA design methodologies: the Switching-Mode (SM) amplifiers [6] or the trans-conductance based amplifiers with Harmonic Tuned terminations (HT) [7]. In the former the active device is driven by a large input signal to act as a switch, rather than as a current source in HT amplifiers. For this reason the resulting SM amplifier are often considered as a \( dc/RF \) converter rather than as a RF amplifier. Different solutions have been proposed, namely Class D or S [8], while the most famous and adopted one results in the Class E amplifier configuration [9]. In such amplifiers the high efficiency condition is achieved by minimizing the overlapping of output voltage and current waveforms.

In HT amplifiers, the active device acts as a current source controlled by the input signal (voltage or current for FET or Bipolar devices respectively). Starting from different quiescent active device bias points, resulting in different output current conduction angles (from \( 2\pi \) to 0) and related nomenclature (from Class A, AB, B to C respectively), the high efficiency condition is achieved exploiting the device non linear behaviour through a suitable selection of both input and output harmonic terminations. In this case the most famous solution is the Class F approach [10,11], while for high frequency applications and taking into account practical limitations on the control of harmonic impedances, several solutions have been successfully proposed [12].

![Fig. 1: RF device technologies, relevant applications, and performance (output power) achieved.](image-url)
A. Switching-Mode Power Amplifiers

This class of amplifiers is characterised by the assumption of an ideal switching mode behaviour for the active devices employed. Starting from the early Class E configuration proposed by Sokal in 1975 [13], several approaches and design solutions were later proposed, as Class D and S [8]. However, the Class E amplifier still remain the most adopted methodology, especially in RF wireless systems, due to its relatively simple scheme, and availability of closed form expressions for its circuit components [14]. The basic amplifier schematic is reported in Fig. 2, even if alternative designs have been proposed [15].

![Class E amplifier scheme.](image)

Drain efficiency of switching-mode amplifiers may theoretically reach 100%, and although many loss mechanisms, such as ohmic and capacitive discharge losses, degrade efficiency in actual realisation, high values have been demonstrated. A 90% has been recorded at HF [16], decreasing up to a 70% at microwave frequencies [17]. The frequency range of applicability of Class E amplifier is however intrinsically limited by the active device switching behaviour, limited by the device roll-off frequency. Moreover, device intrinsic output reactive behaviour (mainly dominated by the output capacitance $C_{out}$), further decreases the frequency range of Class E amplifiers, according to the following relation [18]:

$$f_{\text{max}} = 0.063 \frac{I_{\text{max}}}{V_{\text{BD}} \cdot C_{\text{out}}}$$  \hspace{1cm} (1)

where $I_{\text{max}}$ and $V_{\text{BD}}$ are device maximum output current and breakdown voltage respectively.

Class E design approach has been extended for relatively high frequency applications, taking into account the aforementioned practical frequency limitation [18]: in this case the methodology has been successfully applied for the design of a Class E amplifier for S-Band application, based on the recent and innovative GaN device technology. Measured performance of the realised amplifier are reported in Fig. 3 (photo in the box) at 2.4GHz [18].

![Performance @ 2.4GHz](image)

The performance of the realised Class E amplifier are compared in Fig. 4 with state-of-the-art results reported in literature for S-Band applications (mainly based on CMOS technology).

![Efficiency vs. output power for S-Band Class E state-of-art amplifiers.](image)

From a linearity point of view, SM amplifiers usually do not exhibit satisfactory performance, since the output power is not directly related to the input power, which is only responsible to
drive the device in on-off states. Consequently, SM amplifiers are commonly adopted for constant-envelope modulation schemes, requiring less stringent linearity performance, or in complex architectures like EER (Envelope Elimination and Restoration) and LINC (Linear amplification using Nonlinear Components) [2], where a high efficiency and constant envelope amplifier is required. Recent results shown that Class E amplifier can be successfully applied in transmitter with time-varying envelope operating at X-Band [19].

B. Harmonic Tuned Power Amplifiers

In this class of amplifiers the active device is operated (and modelled) as a current source, whose waveform is mainly controlled by the input driving signal, at least at a first approximation [5]. High efficiency condition is achieved exploiting the active device non linear behaviour (in large signal operating conditions) by a suitable choice of both input and output harmonic terminations, to properly shape the device output current and voltage waveforms [7]. Starting from the pioneering work on Class F amplifier theoretically proposed by Snider in 1967 [20], more realistic and useful solutions have been investigated and proposed, accounting for practical limitation in the number of controlled harmonic terminations [7]. The generic scheme of an HT amplifier is reported in Fig. 5, where in actual realisation the idler are usually replaced by matching networks designed to fulfil well-identified frequency constraints at harmonic frequencies.

![Fig. 5: Theoretical scheme for HT amplifiers.](image)

The disadvantage of HT amplifiers, as compared as to SM amplifiers, is related to the lack of closed form design expressions, even if a theoretical formulation and useful design guidelines have been proposed in [7] and experimentally validated in [21], stressing also the relevance of input harmonic terminations. The HT methodology aims to shape the output voltage waveform to fulfil device physical constraints, while assuring an higher fundamental component as compared as to a standard Class A amplifier. Such amplifiers are classified according to the terminations controlled, like Class F (or 3rd HT), 2nd HT or 2nd & 3rd HT amplifiers. The HT approaches have been applied to design several state-of-the-art amplifiers. For instance, Class F strategy has been adopted to design monolithic microwave integrated circuits (MMIC) PA based on PHEMT GaAs device, for X-Band application (9.6 GHz), investigating and demonstrating the possibility to adopt innovative design criteria to combine active devices, to further increase output power levels, fulfilling HT conditions [22]. The measured performance of the realised Class F amplifiers are reported in Fig. 6 (photo in the box).

![Fig. 6: Measured performance of realised (photo in the box) Class F MMIC PA, based on single (1.5x1.9mm²) and coupled (1.8x2.3mm²) GaAs PHEMT devices](image)

With the advent of GaN devices, characterised by a very high breakdown voltage, the use of a 2nd HT strategy becomes very attractive, due to the larger improvements assured, as compared to a Class F (e.g. 3rd HT) approach. For instance, a C-Band 2nd HT amplifier has been designed in hybrid technology employing a GaN device, whose measured performance at 5.5GHz is reported in Fig. 7 [23].
To demonstrate the promising results, a comparison with other state-of-the-art GaN amplifiers reported in literature is depicted in Fig. 8, resulting in the highest efficiency of 63% achieved with GaN devices.

As described in the previous section, if $P_{\text{out}}$ and $\eta$ performance are concerned, an established solution consists in making use of suitable harmonic tuning strategies, exploiting device non linear behavior [12]. When linearity performance becomes critical, proposed design techniques are based on the identification (and related PA networks design) of the so-called large-signal IMD sweet-spots [24,25], e.g. circuit condition giving rise to a null for the third order intermodulation product (IMD$_3$). Such peculiar nonlinear effects can be qualitatively explained as opposite phase interactions of small- and large-signal IMD components, typically arising from the mild nonlinearities of device output current. Even if IMD sweet spots seems to be related to some design parameters, as device bias voltage (especially input voltage), input power level, temperature and load impedances [26], actually a well-established design approach to maximize C/I$_3$ through IMD sweet spots control has been not yet identified, and key roles are played by designer experience and active device non linear model consistency. As a consequence, linearization techniques, like feedback, feedforward, or predistortion [27,28] are adopted.

Anyway, to optimise PA performance through a linearization scheme, the PA itself has to exhibit a symmetric behavior for its IMD products, to avoid a different compensation requirement (and
related technical hitches) for the lower and upper sidebands of generated IMD signals (varying with input drive and tone spacing also) [29]. Thus many efforts have been recently devoted to investigate non linear mechanisms generating IMD asymmetries in active devices. With a Volterra analysis and assuming a two-tone drive (at frequencies $f_1$ and $f_2$, with $\Delta f = f_2 - f_1$), effects of active device terminations at fundamental and harmonic frequencies were identified [30,31]. In particular, the condition nulling IMD asymmetry ($\Delta IM_3$) was derived, resulting in a purely resistive termination at the device output (drain) port at base-band frequency ($\Delta f$) [30]. Starting from such results, several contributions propose base-band schemes [32] or “ad hoc” drain bias networks [33] minimizing $\Delta IM_3$. Nevertheless, such schemes increase the PA complexity and dimensions, without any minimization effects on the absolute $IM_3$ output level. Starting from the Volterra analysis of a FET device, a new condition to null $\Delta IM_3$ was recently proposed, based on a suitable choice of both fundamental and second harmonic output terminations, also in agreement with harmonic tuning approaches [34]. In particular, the inferred condition implies output network synthesis to realize a purely resistive terminations at fundamental and second harmonic frequencies, at the device output intrinsic current source, in spite of controlling the network base-band behavior.

V. SOLUTION TO IMPROVE PA PERFORMANCE

The increasing request to transmit a growing amount of information on the same transmission channel resources, has pushed towards the development of complex modulations techniques (WCDMA, UMTS, etc), resulting in severe requirements in terms of linearity, mainly demanded to the electronic front-end. Moreover, the scenario is further complicated by the time-varying envelope signals behaviour, with typical peak-to-average power ratio between 6 to 12 dB, resulting in a decrease of performance evaluated in terms of time average rather than peaking levels. As a consequence, some old-fashioned solutions have been recently resurrected to overcome the drawbacks related to these kind of signals. In particular, two main strategies have been revisited, namely the Doherty [35] and the Envelope Tracking (ET) techniques [36]. The former exploits the concept of a dynamic load while the latter implies dynamic bias conditions, both with the aim to force the amplifier stage to operate at maximum efficiency levels for a predefined input dynamic range.

A. Doherty Amplifier

Such a technique, introduced for the first time in 1936 by Doherty [35], is based on the dynamic modulation of the load presented to a given device by using the active load pull concept. The basic scheme is depicted in Fig. 10, where the Aux amplifier is deputised to modify the load of the Main amplifier, through the output quarter-wave Transmission Line (TL), when the last reaches its saturation (e.g. maximum efficiency) operating condition.

Simplifying the description, for low input drive levels the Aux amplifier is turned off, and the Main amplifier is loaded by an impedance doubled with respect to the required optimum value $R_{opt}$, due to the quarter line transformation. When the Main amplifier starts to saturate, resulting in the load curve $LC_1$ in Fig. 11, the Aux amplifier is turned on, and the electrical situation becomes the one depicted in Fig. 12.
Fig. 11: Load curves of Main and Auxiliary amplifiers in a Doherty configuration.

Thus the Aux amplifier modifies the load of the Main amplifier through the following relationship:

$$R_{\text{Main}} = \frac{Z^2}{R_L \left(1 + \frac{I_{\text{Aux}}}{I_2}\right)}$$ (2)

At the end, both amplifiers reach their final saturation conditions, corresponding to the load curves LC2 and LC3 for the Main and Aux amplifiers respectively (Fig. 11).

Theoretical drain efficiency resulting from the overall structure is reported in Fig. 13, for several choices of the parameter $\alpha$, related to the current (as percentage of maximum value) reached by the Main amplifier when the Aux is turned on (see Fig. 11).

Trends for output power and PAE reported in literature in the last three years for Doherty amplifiers used in CMDA applications in the range of 1950-2170 MHz are depicted in Fig. 14, showing an increase in efficiency requests rather than in output power levels.

B. Envelope Tracking

ET technique [36] or, in general terms, polar modulation techniques [37], are based on the dynamic modification of the device bias to attain maximum efficiency for each input signal drive. The basic scheme is reported in Fig. 15, where the envelope amplifier (EA) is aimed to bias the main amplifier to operate roughly at 1dB compression for a fixed input drive.

The major issues of ET technique is related to the practical implementation of the envelope amplifier, required to act as an high efficiency $dc/dc$ converter, not to decrease overall system efficiency. The major issue is represented by the
bandwidth required to EA, according to modern modulation schemes (WCDMA, UMTS, etc.), to avoid distortion phenomena. Several solutions have been proposed based on buck converter configuration [38], and actually two positions seem to be identified, respectively the Wide Bandwidth Envelope Tracking (WBET) or the Average Envelope Tracking (AET). WBET scheme tracks the instantaneous wide-bandwidth input envelope signal power, whereas the AET scheme follows the long-term average input envelope signal power [39].

Theoretical efficiency performance as a function of the output power is reported and compared in Fig. 16, for different amplifier configurations or architectures [40].

![Fig. 16: Efficiency vs. output power for different idealized amplifier architectures, including Class A, Class B, Doherty and ET.](image)

In principle both Doherty and ET techniques could assure the highest average efficiency for a large output dynamic range. However, from a practical point of view, main drawbacks of Doherty amplifiers are related to their intrinsic bandwidth limitation, related to the quarter line required for the active load pull concept. For the ET technique, the major weakness are related to the dc/dc converter efficiency performance, affecting overall efficiency and overriding theoretical improvement achievable with the PA bias control.

VI. CONCLUSIONS

In this contribution an overview of main research activities performed in the field of RF and microwave power amplifiers design have been discussed. Starting from a review of PA design strategies, the results achieved by TARGET activities have been presented, providing state-of-the-art amplifier performance, by using GaAs or GaN technologies and different design strategies. Finally, some re-discovered amplifier architectures (Doherty and ET) have been discussed identifying a potential future trend in PA design.

VII. ACKNOWLEDGMENTS

Research reported here has been partially performed in the context of the network TARGET- "Top Amplifier Research Groups in a European Team" and supported by the Information Society Technologies Programme of the EU under contract IST-1-507893-NOE, www.target-org.net.

VIII. REFERENCES


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