Design of a C-Band Versatile and Low Cost Oscillator for Satellite Applications
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Abstract- A C-band bipolar oscillator designed by the method of negative resistance is presented. The output frequency can be simply changed by changing the length of an open stub. It is possible to modify also the sweep frequency versus the controlled voltage by changing a capacitor. Featured by space-qualified and simple assembly, a prototype has been realized and fully characterized in order to evaluate its performance. A good stability versus temperature has been reached. The output power is 10dBm, split between two outputs. The sweep frequency is about 500MHz. The phase noise is -105dBc/Hz@100KHz.

Index Terms- C-Band Oscillator, Phase Noise, Resonator, VCO.

I. INTRODUCTION

Wideband tunable oscillators are important components in many electronics systems. Resonators with high quality factor (dielectric or coaxial resonator) are usually used to obtain low phase noise oscillators. A typical C-band satellite application adopts the 3.7–4.2GHz band in downlink [1]. At these frequencies the dielectric or coaxial resonator are very large and difficult to integrate so it is preferable to achieve a low phase noise oscillator.

In this paper a design of a C-Band versatile and low cost oscillator for satellite applications will be presented. The main concepts underlying the design of oscillators are remembered and all oscillator parts will be analyzed one by one. Test results are also shown.

In the design a particular attention has been posed on the output power and the phase noise.

II. THEORY OF OPERATION

In oscillator design, feedback is often applied in order to increase the negative resistance of the transistor. A block diagram of an oscillator is shown in Figure 1. The active device is characterized by its S parameters.

![Oscillator block diagram](image)

Figure 1: Oscillator block diagram

\( \Gamma_s(\omega) \) and \( \Gamma_i(\omega) \) represent the reflection coefficients of the resonator circuit and the output matching network. \( \Gamma_D^{\text{in}}(V, \omega) \) and \( \Gamma_D^{\text{out}}(V, \omega) \) are the reflection coefficients at the active device input and output respectively.

Embedding the resonator, whose impedance is \( Z_R(\omega) = R_s(\omega) + j \cdot X_s(\omega) \), into the active device block, allows representing the two-port network as a one-port negative-resistance device. The output impedance of this one-port device is \( Z_D^{\text{out}}(V, \omega) = R_D^{\text{out}}(V, \omega) + j \cdot X_D^{\text{out}}(V, \omega) \) (Figure 2).

In this condition, \( \Gamma_D^{\text{out}}(V, \omega) \geq 1 \), thus exhibiting a negative real part for its admittance. In this way, a compact representation of the oscillator is obtained.
The oscillation condition is to be verified at each oscillator section; in particular, at the active device input and output ports. The two conditions below must hold:

\[
\Gamma^\text{IN}_D(V, \omega) \cdot \Gamma_L(\omega) = 1 \\
\Gamma^\text{OUT}_D(V, \omega) \cdot \Gamma_L(\omega) = 1
\]

In the case of a series resonance condition, it is convenient to express the oscillation condition in impedance domain. Thus (2) becomes:

\[
Z^\text{OUT}_D(V, \omega) + Z_L(\omega) = 0
\]

i.e., showing real and imaginary parts,

\[
R^\text{OUT}_D(V, \omega) + R_L(\omega) = 0 \\
X^\text{OUT}_D(V, \omega) + X_L(\omega) = 0
\]

During oscillation start-up, condition (4) transforms into the condition:

\[
R^\text{OUT}_D(V, \omega) + R_L(\omega) < 0
\]

The load resistance is generally selected as:

\[
|R^\text{OUT}_D(V, \omega)| \geq 3 \cdot R_L(\omega)
\]

(Gonzalez [4] suggests this rule to maximize oscillator output power). If a nonlinear device model is available, the optimum load for the oscillator can be found by simply searching the Smith chart via a simulated load-pull procedure. Through the output network, the load impedance \(R_L\) can be transformed into an appropriate impedance \(Z_L(\omega) = R_L(\omega) + j \cdot X_L(\omega)\), verifying equations (5) and (6).

As the oscillation amplitude increases, the negative resistance decrease, transforming (6) into (4).

Conditions expressed by (4) and (5) are not sufficient to guarantee a stable oscillation since \(X^\text{OUT}_D(V, \omega)\) is a voltage dependent quantity, typically leading to an oscillation frequency, \(\omega_0\) different from the start-up one, i.e.:

\[
X^\text{OUT}_D(V, \omega) \neq X^\text{OUT}_D(V_s, \omega_0)
\]

If \(X^\text{OUT}_D(V, \omega)\) frequency dependence can be neglected, for small variations around \(\omega_0\), it can be shown that a stable oscillation can be achieved if:

\[
\left. \frac{\partial R^\text{OUT}_D(V, \omega)}{\partial V} \right|_{V=V_s} \left. \frac{\partial X_L(\omega)}{\partial \omega} \right|_{\omega=\omega_0} > 0
\]

Generally, the last term is pretty small (above all if an output matching network is not present since, in this case, \(R_L(\omega)=R_0\) is held constant) and equation (9) can be consequently simplified [3], [4], [5].

\[
\left. \frac{\partial R^\text{OUT}_D(V, \omega)}{\partial V} \right|_{V=V_s} \left. \frac{\partial X_L(\omega)}{\partial \omega} \right|_{\omega=\omega_0} > 0
\]

III. ACTIVE DEVICE BIAS

In Figure 3, the DC biasing scheme adopted for the active device is reported:

\[
\begin{align*}
R_2 & \quad R_3 & \quad R_0 \\
V_s & \quad & \quad V_C \\
V_b & \quad V_C & \quad V_{CC} \\
V_E & \quad & \quad R_E
\end{align*}
\]

Figure 3: Bias circuit of the oscillator
This BJT oscillator makes use of a 4 bias resistors configuration: such topology assures a stable performance as a function of temperature variations. The collector voltage is fixed to 4V. For a negligible $I_b$, the collector current can be simply obtained by:

$$V_C = V_{CC} - R_C \cdot I_C$$  \hspace{1cm} (11)$$

$$V_B = V_C \cdot \frac{R_2}{R_1 + R_2} \quad (\text{with } I_B \approx 0)$$  \hspace{1cm} (12)$$

$$I_C \approx \frac{V_L}{I_E} \approx \frac{R_1 + R_2}{R_E \cdot (R_1 + R_2) + R_c \cdot R_2} \cdot \left( \frac{R_2 \cdot V_{CC}}{R_1 + R_2} - V_B \right)$$  \hspace{1cm} (13)$$

Temperature has a strong effect only on $V_{BE}$, so that $V_{BE} = V_{BE}(T)$. In this case:

$$\frac{\partial I_C}{\partial T} \approx - \frac{R_1 + R_2}{R_E \cdot (R_1 + R_2) + R_c \cdot R_2} \cdot \frac{\partial V_{BE}(T)}{\partial T}$$  \hspace{1cm} (14)$$

With the components used ($R_1 = 1\, \Omega$, $R_2 = 0.65\, \Omega$, $R_c = R_e = 20\, \Omega$ and $V_{CC} = 4V$), the operating point can be evaluated as:

$$I_C \approx \frac{R_1 + R_2}{R_E \cdot (R_1 + R_2) + R_c \cdot R_2} \cdot \left( \frac{R_2 \cdot V_{CC}}{R_1 + R_2} - V_{BE} \right) \approx 31.4mA$$  \hspace{1cm} (15)$$

$$V_{CEO} = V_{CC} - (R_C + R_E) \cdot I_{CO} \approx 2.74V$$  \hspace{1cm} (16)$$

For many BJTs, it can be assumed that:

$$\frac{\partial V_{BE}(T)}{\partial T} \approx -2mV/\degree C$$  \hspace{1cm} (17)$$

and then:

$$\frac{\partial I_C}{\partial T} \approx - \frac{R_1 + R_2}{R_E \cdot (R_1 + R_2) + R_c \cdot R_2} \cdot \frac{\partial V_{BE}(T)}{\partial T} \approx 71\mu A/\degree C$$  \hspace{1cm} (18)$$

IV. RESONATOR DESIGN

The adopted resonator scheme is composed by an open stub, a varactor and an additional capacitor. Also the input nonlinear capacitance of the active device (essentially $C_{ae}$) influences the resonator. So the resonator equivalent representation becomes the one shown in Figure 4.

Figure 4: Resonator equivalent representation

So, if temperature changes from -35°C to +75°C (as specified for satellite applications), the collector current changes by about 7.8mA only.

A temperature change, a bias voltage variation or simply the noise effect, acts on the device nonlinear capacitor value, therefore affecting the oscillation frequency:

$$\frac{\partial \omega_n}{\partial C_{NL}} = - \frac{1}{2 \cdot \left( C_{NL} \right)^2 \cdot L \cdot \left( \frac{1}{C} + \frac{1}{C_{VAR}} + \frac{1}{C_{NL}} \right)^2}$$  \hspace{1cm} (18)$$

$L$ = Open stub equivalent inductance

$C$ = Capacitor

$C_{VAR}$ = Varactor

$C_{NL}$ = Device nonlinear capacitance
If $C$ decreases, such frequency sensitivity on the nonlinear capacitor is reduced accordingly. This is a very good strategy if a free-running oscillator has to be designed, since device changes do not impact on the operating frequency [2]. In this case unfortunately, the sensitivity on the varactor variation is also reduced: if a voltage controlled oscillator has to be designed, such strategy cannot be adopted. The capacitor value has to be therefore selected in order to obtain a balance between the desired sweep frequency and the minimum variation due to the device parasitics.

V. ACTIVE DEVICE AND FEEDBACK

In this oscillator the BJT BFY193 manufactured by Infineon is used. The SPICE nonlinear model used for this device is a Gummel Poon one, implemented in Berkley-SPICE 2G.6 Syntax, whose parameters are reported in Table 1.

The transistor used to realize an oscillator is often not unstable at the design frequency, and thus the transistor stability condition can be varied by an external feedback. For the adopted common emitter configuration, a capacitor connected from emitter to ground is typically used. In the designed oscillator, the open stub shorter than $\lambda/4$ on emitter is equivalent to a feedback capacitor (Table 1).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>BEF</td>
<td>24</td>
</tr>
<tr>
<td>BAF</td>
<td>2.0549</td>
</tr>
<tr>
<td>NEF</td>
<td>1.4288</td>
</tr>
<tr>
<td>VAR</td>
<td>2.03725</td>
</tr>
<tr>
<td>NC</td>
<td>1.8368</td>
</tr>
<tr>
<td>RBE</td>
<td>0.76634</td>
</tr>
<tr>
<td>CJE</td>
<td>1.1524</td>
</tr>
<tr>
<td>TFE</td>
<td>18.828</td>
</tr>
<tr>
<td>VUC</td>
<td>1.1528</td>
</tr>
<tr>
<td>TR</td>
<td>1.0037</td>
</tr>
<tr>
<td>EPS</td>
<td>0.75</td>
</tr>
<tr>
<td>XTI</td>
<td>1.11</td>
</tr>
</tbody>
</table>

Table 1: Transistor Chip Model Parameters

The “output matching network” transforms the load impedance, providing an optimum load at oscillator’s output. The optimum load is not the complex conjugate, but a load designed in order to obtain the maximum output power, the best phase noise or the maximum efficiency.

With the resonator connected to the base terminal and the feedback on the emitter one, the device collector exhibits an impedance with a negative real part. We have to keep in mind equation (9) in order to correctly evaluate the system performance. An impedance with a large negative real part is not sufficient to guarantee a stable oscillation since the impedance imaginary part should exhibit the proper phase variation.

The output network is then tuned to obtain the simultaneous fulfillment of equations (5), (6) and (9).

As it can be noted in the following, the equation for the oscillation start-up can be easily fulfilled.
since many possible values for $R_L(\omega)$ can be selected:

$$|R_{D}^{\text{OUT}}(\omega)| > R_L(\omega)$$

As already stated, to obtain maximum output power, Gonzalez [4] suggest:

$$|R_{D}^{\text{OUT}}(\omega)| > 3 \cdot R_L(\omega)$$

However, a different optimum load can be selected in order to reach a better phase noise performance or an higher efficiency.

VII. OSCILLATOR SCHEMATIC

The overall oscillator scheme is reported below.

![Overall Oscillator Schematic](image)

Figure 6: Overall Oscillator Schematic

In Figure 6 all the subcircuits are indicated. This oscillator has two outputs, so to be easily adopted within a PLL scheme. The first output ($P_{\text{OUT1}}$) is the main one, while the second output ($P_{\text{OUT2}}$) can be connected to the phase detector in the PLL arrangement.

VIII. TEST RESULTS

In the Figure 7 the resulting oscillator assembly is reported.

![Realized Oscillator Assembly](image)

Figure 7: Realized Oscillator Assembly

In the Table 2 the variation of the collector current versus temperature is reported. As can be seen, if the temperature change is 110°C the current change is about 7.1mA. By using equation (18), an estimate of such variation can be performed, resulting in about 7.8mA predicted variation.

<table>
<thead>
<tr>
<th>Collector current vs Temperature</th>
<th>T = -35°C</th>
<th>T = -25°C</th>
<th>T = -75°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I$ (mA)</td>
<td>20.7 mA</td>
<td>32.6 mA</td>
<td>55.8 mA</td>
</tr>
</tbody>
</table>

Table 2: Bias variation as a function of temperature

In Figure 8 the output spectrum, measured full span, is reported. The oscillation frequency is 4GHz. The output power (at the output port 1) is about 7.5dBm, resulting in a total oscillator output power about 10.5dBm. The distance between the carrier and its second harmonic is higher than 30dBc.

![Output spectrum of the oscillator](image)

Figure 8: Output spectrum of the oscillator
In Figure 9 the frequency variation obtained by changing the control voltage from 0V to 10V is shown. In any condition the output power variation is less than 1dBpp.

![Figure 9: Sweep frequency as a function of the control voltage](image)

In Figure 10 the phase noise measured at 100KHz from the carrier is reported. The phase noise is -105dBc/Hz@100KHz: such noise level is considered more than adequate for many space applications, for which a typical specified level is -95dBc/Hz@100KHz.

![Figure 10: Measured Phase Noise of the realized oscillator](image)

In this paper the design of a C-Band oscillator for satellite applications has been described. The oscillator has been realized and a full characterization has been reported. The particular bias network used has guaranteed a good stability of the collector current versus the temperature variation. The measured output power is higher than 10dBm, split between the two outputs. The associated phase noise is -105dBc/Hz@100KHz, a more than adequate level for the majority of space applications.

**REFERENCES**


