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Measurement Infrastructure for Optimization and Characterization of Microwave Transistor Devices

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***Abstract*— various techniques and methods have evolved recently for the characterization and measurement of microwave devices. Waveform measurement and engineering system among them is a very promising candidate for the optimization and characterization of transistor device for use in power amplifier design. This paper presents an all encompassing waveform measurement and engineering system which is capable of providing accurate characterization data for the purpose of optimizing the device. The waveform measurement is achieved by applying enhanced calibration algorithm around an MTA based setup. The capability to engineer the waveforms is achieved by an emerging active load pull approach called 'Envelope Load Pull'.**

***Index Terms*— Microwave Device Measurement and Characterization, Active Envelope Load-Pull, Waveform Measurement, Waveform Engineering**

I. INTRODUCTION

Characterization of microwave transistor devices prior to their deployment in the design of power amplifiers (PA) are gaining importance. It serves many purposes, on one hand it helps in collection of data for nonlinear modelling [1-5] to improve the yield, while on the other it helps in first-pass optimal design of PAs [6-9].

Much of today's characterizations of non-linear devices are still carried out using only linear s-parameter measurements [10] measured by Vector Network Analyzer [11]. But such measurements and characterization are far from ideal [12] for insight of the device behavior under nonlinear mode of operation. Due to this reason, the last two decade has experienced the emergence of several variants of Large Signal Network Analyzer [13-16] as they can measure the device parameters under large signal conditions and thus provide valuable insight into device behavior in the non-linear domain.

Time-domain waveform measurement systems [17-20] are very useful tools due to two main reasons. Firstly, much of the fundamental electronic theory based around time domain waveforms, albeit at lower frequencies, is equally valid at high frequencies. Secondly, the ability to analyse the shape of the current and voltage waveforms can form a vital part of the design process. These systems complement the pioneering mathematical analysis [21] that explains the relationship of current and voltage waveforms in obtaining high output power and efficiency from a transistor device. It has also been established that the control of current and voltage waveforms at the device ports can extract higher efficiencies from the designed PAs [22-23]. The experimental technique of waveform control is called waveform engineering [24] that is achieved by incorporating load-pull setup [25-29] in the waveform measurement systems.

This paper elaborates on the development of a waveform engineering system that incorporates the Microwave Transition Analyzer (MTA) based waveform system reported in [18] and the envelope load-pull (ELP) reported in [30]. At first the system is explained and subsequently brief idea of system calibration is given. Finally some unique features of the waveform engineering setup are presented which are then utilized to demonstrate some of the unique measurement applications.

II. SYSTEM DESCRIPTION

A generic block diagram of the waveform measurement and engineering system is depicted in Fig. 1. The system is built around a 2-channel MTA, which is a broadband harmonic receiver, with a capability to capture signals of frequencies up to 40 GHz. The MTA is employed for the measurement of four traveling waves a_1, b_1, a_2 and b_2.

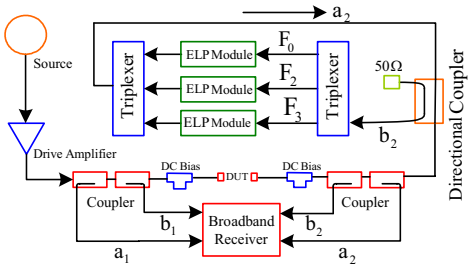

Fig. 1. Generic block diagram of MTA based large signal time domain 3-harmonic waveform measurement and engineering system

Any standard commercial signal generator can work as a source. The drive amplifier at the input ensures that the transistor devices get sufficient drive power for the desired operation. The couplers at the input and output ports are used for the purpose of sensing of the four traveling waves. The Bias-T at the input and output ports supplies the gate and drain voltages to the transistor devices. There are four traveling waves and two channels in the MTA therefore switches are employed, not shown, in the setup so that one measurement shot captures the input waves a_1 and b_1 while the second measurement shot captures the output waves a_2 and b_2. Finally, the ELP block [30] at the output port is employed for the purpose of synthesizing variable load impedance environment.

The architecture of the ELP module is given in Fig. 2. The directional coupler separates the traveling waves a_2 and b_2. The variable impedance, obtained by varying the control variables X and Y, generates family of voltage and current waveforms. Then the selection of appropriate waveforms for the desired power added efficiency (PAE), Output Power (P_{out}) and gain determines the load impedance. Similar architecture can be used at the input for synthesis of variable source impedances. This paper only deals with the waveform measurement setup and the load-pull block.

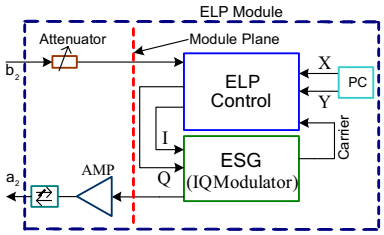

Fig. 2. The block diagram of the ELP module

I. SYSTEM CALIBRATION

A. *Measurement Setup Calibration*

The commercially available transistor devices utilized for illustration purposes in this chapter are mounted on fixture and therefore the need of calibration arises so that the measurement reference plane can be shifted from sampler to the device package plane. The calibration will account for the systematic errors occurring due to imperfections in the MTA, test set, couplers, switches etc. This calibration will not correct for the random errors introduced due to repeatability problems in the instrument and the drift errors which are dependent on environmental factors such as variation in temperature. Although different approaches such as SOLT, TRL/LRL etc can be adopted to calibrate the system but for on fixture device the Thru-Reflect-Line (TRL) [31] technique is more accurate calibration procedures as it only relies on the knowledge of impedance of the lines, requiring no definitions.

The lines employed in the current illustration have ratings of *0.2-3* GHz and *2-20* GHz, these can both be used in a double line calibration in order to calibrate from 0.2 up to 20 GHz. The 8-term error model [26] to calibrate the measurement system [18] is depicted in Fig. 3, given at the end. The terms e_{00}, e_{10}, e_{11} and e_{01}

accounts for the errors at the input port of the DUT whereas e_{22}, e_{32}, e_{33} and e_{23} accounts for the output port.

The approach adopted to calibrate the system is two-tier. The first tier is the s-parameter calibration, also called small signal calibration, is based on the ratio of travelling waves meaning only relative measurements are calibrated leaving the absolute power associated with the waves un-calibrated. The second tier is the large signal calibration, also called full calibration [24], in which the absolute values of parameters e_{10} and e_{01} are ascertained. The measurement of these parameters helps in the absolute measurements of the travelling waves. The two-tier calibration helps in the correct determination of absolute magnitude and phase of the travelling waves, a_1, b_1, a_2, and b_2, at the DUT plane given by:

$$a_1 = a_0 \times e_{10} + b_1 \times e_{11} \tag{1}$$

$$b_1 = \frac{b_0 - e_{00} \times a_0}{e_{01}} \tag{2}$$

$$a_2 = a_3 \times e_{23} + b_2 \times e_{22} \tag{3}$$

$$b_2 = \frac{b_3 - e_{33} \times a_3}{e_{32}} \tag{4}$$

Once the measurement system is calibrated, the ELP modules need to be calibrated before they are employed in the measurement applications. The next section briefly discusses the calibration of ELP modules.

B. Envelope Load-Pull Calibration

The standard commercial components have been employed in the design of ELP modules and therefore appropriate calibration strategy [25] is required to nullify any imperfections introduced by these components. The error model to remove the imperfections in the ELP setup reported in [25] is being reproduced in Fig. 4. In the error model, the factor T_d and T_m refers to the imperfections in the respective demodulator and modulator, D and M refers to the dc-offset in the demodulator and the modulator respectively, Γ_0 refers to the system passive impedance, Γ_f refers to the feedback effect while Γ_{set} is the load controlled by the computer.

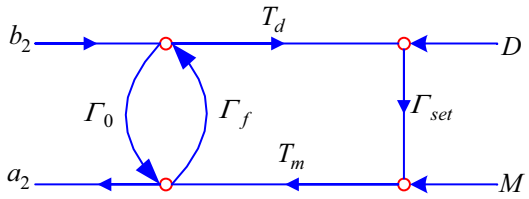

Fig. 4. Error flow model of envelope load-pull setup

In ideal situation, with no imperfections in the components, the load $\Gamma_{set}=X+jY$ set by the ELP module should be equal to the desired load, Γ_{load}, at the reference plane. But the imperfections in the components, defined by the error model in Fig. 4, establish the following relationship:

$$\Gamma_{Load} = \frac{a_2}{b_2} = \left(\frac{\Gamma_{set} T_d T_m}{1 - \Gamma_f (\Gamma_{set} T_d T_m)} + \Gamma_0 \right) \tag{5}$$

The dc-offset terms D and M are eliminated by deploying high-pass filters in the ELP module [25]. The designed ELP is then integrated in the measurement system and the desired impedance data set, regulated by computer controlled variables X and Y, is defined for calibrating the setup and the measurement system is operated on a THRU standard without employing the ELP error model. This measures the un-calibrated impedance data set which is not exactly the one desired but is a function of desired impedance data set as demonstrated in Fig. 5. As per equation (5), there are three unknowns T_dT_m, Γ_0 and Γ_f, and hence requires at least three data points in the desired Γ_{set} to determine these unknown parameters. Although the accuracy in the calibration improves by increasing the data points in the desired Γ_{set}, but a set of *15-20* points achieves very good accuracy [25]. This trade-off in the accuracy and number of calibration points is also regulated by the calibration speed.

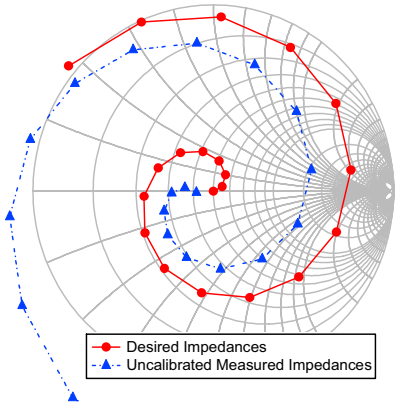

Fig. 5. The desired and un-calibrated measured impedance points during ELP calibration

The measured un-calibrated data points are then compared to determine the error parameters T_d, T_m and Γ_f and then the measurement system is operated by incorporating the error model in the measurement automation software. The obtained result is shown in Fig. 6 that clearly demonstrates that the 20 point calibration sequence is able to correct the impedance presented by the ELP module.

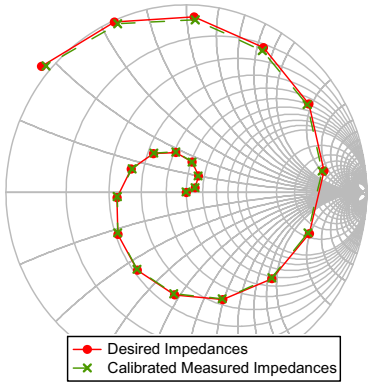

Fig. 6. The desired and calibrated measured impedance points during ELP calibration

The 20 points calibration process, typically, takes less than 10 minutes for one ELP module which comes out to be less than 30 minutes to calibrate the 3-harmonic ELP system shown in Fig. 1. A very interesting outcome is observed when the calibration process is repeated for *3* points, *10* points, *12* points and *30* points calibration data set. The results reveal that the accuracy in the ELP calibration is not that much dependent on the number of calibration points once the load points in the calibration data set is above *12*.

Thus to expedite the measurement process and the measurement throughput the load points in the calibration data set could be chosen based on the applications. It is important to note that there is no earlier report of calibration of other active load-pull setups and the commercial passive load-pull setups need at least *500-700* points for achieving substantial accuracy in the calibration [32].

IV. FEATURES OF THE SYSTEM

The waveform measurement system based around 2-channle MTA is capable of measuring the current and voltage waveforms at the DUT reference plane. The easy and flexible calibration of the system provides the possibility of fast measurement throughput.

The integration of the ELP modules in the waveform measurement system allows the engineering of waveforms at the DUT output port. The ELP calibration is fast and thus has advantage over the passive load-pull setup when comparing the measurement throughput. Additionally, the ELP is based on the active technique and therefore is capable of synthesizing load impedances over entire smith chart.

The ELP setup can synthesize load impedances which are independent of changes in the drive power, device bias conditions or operating frequency. The ELP is also capable of synthesizing harmonically independent load impedances [30]. These features make the ELP a very promising candidate to augment the existing industry adopted passive load pull systems.

V. MEASUREMENT APPLICATIONS

All measurement data presented within this section is obtained at the ‘package plane’ of the

fixture. This is described as the point at which the bond wires are attached to the Thin Film Networks (TFNs), in the centre of the vertical gold stub carriers as shown in Fig.7.

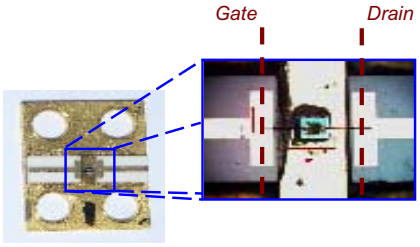

Fig. 7. Package reference plane location

The device used in the current measurement investigation is *1W GaAs pHEMT*. Prior to the RF investigation, static DC-IV measurements were taken over the gate voltage range of *-1.1V* to *0V* in *0.1V* steps and to $V_d = 8V$. The DC-IV is displayed in Fig. 8, with a power compliance of *800mW*, after the drain-feed series resistance has been taken into account. From this, and further DC measurements it was found that this device had a pinch-off of $V_{gs} = -1.2V$ ($I_{dq} \approx 1mA$) and $I_{dss} = 300mA$.

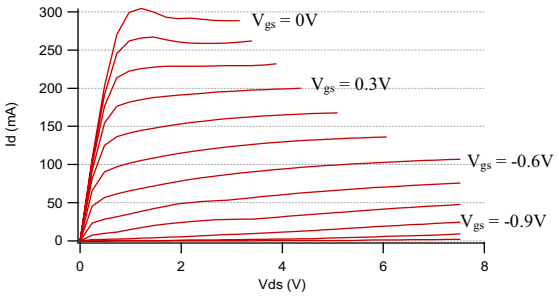

Fig. 8: DC-IV characteristic of 1W GaAs pHEMT

The device was then biased in Class-B by setting $V_{gs} = -1.2V$ ($I_{dq} \approx 1mA$) and $V_d = 10V$ and the measurement system was set to operate at a fundamental frequency, F_1, of *900 MHz*. Then the fundamental output impedance of the device, $Z(F_1)$, was swept over a *64*-point grid, whilst the second harmonic was held to a package plane short, $Z(F_2) = 1\angle 180^o$, and the third harmonic impedance, $Z(F_3)$, being held to an arbitrary value of *15Ω*. The input power, P_{in}, was held at *12.8 dBm*. The output power contours for the *64*-point impedance grid is given in Fig. 9. The rapid nature of the ELP based measurement system enabled this measurement in less than *30* mins. It is evident that the maximum output power for this device is roughly *30.4 dBm* for which the optimal fundamental impedance, $Z(F_1)$, comes out to be *33.9+j2.8Ω*.

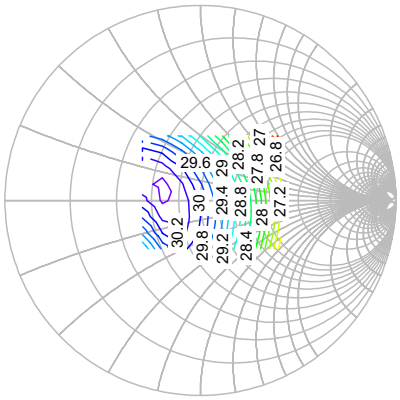

Fig. 9. Load-Pull Contours at P_{in} = 12.8dBm for the 64-point impedance grid

The rapid and harmonically independent impedance synthesis features of the ELP setup can also be utilized in determining the sensitivity of harmonic impedances on the device performance. For this purpose, the $Z(F_1)$ was set to *33.9+j2.8Ω* and a phase sweep around the edge of the Smith chart for $Z(F_2)$ was carried out to quantify the effect of second harmonic on the device performance while terminating $Z(F_3)$ to *15Ω*.

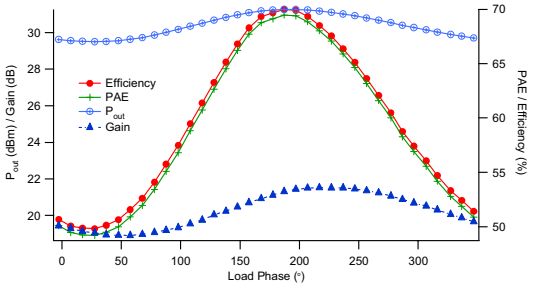

Fig 10. The dependence of device performance on the second harmonic load impedance

It can be extracted from the achieved result in Fig. 10 that the output power varies between *29.50-31.27dBm*, efficiency varies between *49.82-69.97%* and gain varies between *18.90-21.51dB* as the phase of $Z(F_2)$ was swept from 0-360°. It is also evident the optimal $Z(F_2)$ for this device is $1 \angle 188^{o}$ *(-j3.5Ω)*.

The coupling of waveform measurement system [18] and the ELP setup [25] could also be used for monitoring the shape of terminal current and voltage waveforms, and at the same time in the determination of device performance in power sweep applications. The device was once again biased in class-B and the drive power was swept at *16* different levels between *-5* to *15 dBm*. The results in Fig. 11 provide the device performance as a result of the power sweep. The plot clearly identifies all the standard parameters and could also be used for the determination of other parameters such as 1-dB compression point; dual-inflection point in GaAs based devices etc.

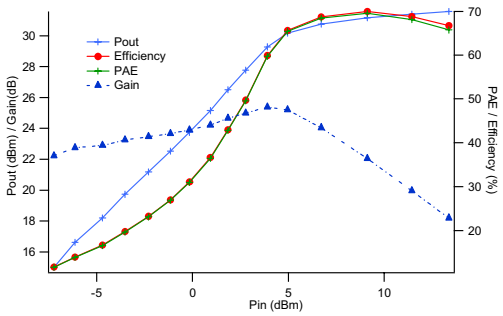

Fig. 11. Input power sweep at loaded optimal impedances

The terminal waveforms at the output port resulting from the power sweep are given in Fig. 12 and Fig. 13. The waveforms clearly show that the device has been biased in class-B. The waveforms slightly overlap due to the parasitic effect in the packaging of the device. The de-embedding of the waveforms to current generator plane will remove this overlap. Thus the waveform measurement and engineering system finds the usage in the characterization, optimization and design of microwave devices and power amplifiers.

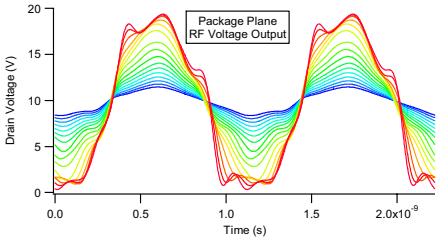

Fig. 12. RF output voltage waveforms for each measured input power point

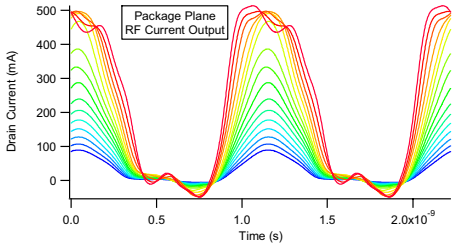

Fig. 13. RF output current waveforms for each measured input power point

The waveform measurement and engineering systems could also be used in examining the effect of DC-RF dispersion, which can lead to "knee walkout" and "current collapse", especially within GaN technology devices, that can limit the power output and efficiency ratings. This is qualified by the actual observed RF waveforms experiencing premature compression when compared to the DC characteristics of the device. In order to quantify this phenomenon, the DC-IVs can be compared to RF 'fan'-diagrams. A 'fan'-diagram is produced by driving the device and output waveforms into compression for a number of fundamental load impedances in order that the dynamic load lines trace out the RF boundary.

'Fan'-diagrams were traced out for a range of *13* load-lines measured at V_d *=10V* for a *500mW* GaN FET device. Fig. 14 shows the case where the $Z(F_1)$ were altered whilst actively holding $Z(F_2)$ and $Z(F_3)$ to *50Ω*. Whereas Fig. 15 demonstrates the same fundamental sweep, but with the harmonics being held to short. It can be seen from both fan diagrams that the device does

suffer from slight knee walkout, with larger knee voltages than indicated through the DC-IVs.

This is important information to the PA designer, especially when trying to avoid interaction with the knee, such as with main Doherty device design. It is interesting to note though that the boundary traced out when the harmonics are terminated into shorts is more pronounced than into *50Ω*. This implies that should it be required that the device be biased in a Class-B manner, shorting the harmonics, the operation space is further reduced than given in the DC-IV's.

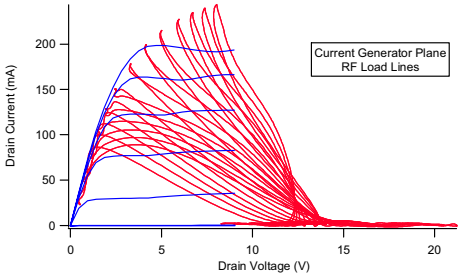

Fig. 14. Dynamic load-lines of fan diagram at V_d = 10V, measured while holding the second and third harmonic impedances actively at 50Ω

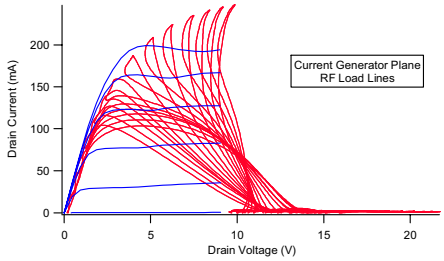

Fig. 15. Dynamic load-lines of fan diagram at V_d = 10V, measured while holding the second and third harmonic impedances actively at short

The above analysis requires setting of various harmonic load impedances and ELP system is ideally suited for such situation due to its unique features. The coupling of ELP to the waveform measurement system expedites the measurement throughput by a great deal of time.

VI. CONCLUSION

This paper has underlined the usefulness of waveform measurement and engineering systems in the device characterization, optimization and design. This paper also outlines the benefits one could achieve by combining the waveform measurement systems and the rapidly emerging ELP systems.

It has been shown that a calibrated waveform measurement system aids in the speedy calibration of the ELP modules. Through rigorous measurement examples it has been demonstrated that the fast and harmonically independent impedance synthesis feature of ELP can be employed in fully characterizing the microwave devices. Therefore it could be concluded that the waveform measurement systems coupled with ELP systems could become extremely useful in the optimization and design of microwave devices and power amplifiers.

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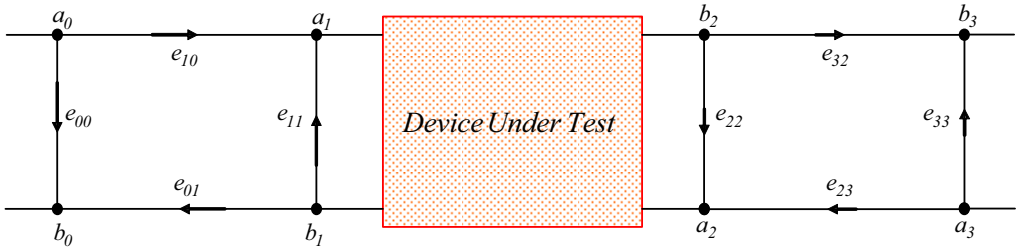

Fig. 3. Measurement system error model for correct reference plane definition