



Microwave Phase Shifter with Electromagnetic Signal Coupling in Silicon Bulk Technology

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Abstract- This contribution presents a Distributed MEMS Transmission Line (DMTL) phase shifter for the 24 GHz ISM band fabricated in silicon bulk technology. Using this technology enables the suspension of all capacitive loads on one movable plate and therefore allows wide range analog and homogeneous tuning. To avoid commonly used metallic feed-throughs for signal connection, an electromagnetic signal coupler guides the microwave signal non-galvanically from printed circuit board level, through the chip substrate into the MEMS device. The first available prototypes of the phase shifter are characterized to provide 50°/dB loss normalized differential phase shift at 24 GHz. The achievable normalized insertion loss of the coupling structure has been determined with 0.13 - 0.17 dB.

Index Terms- RF-MEMS, phase shifter, coupler, coplanar waveguide.

I. INTRODUCTION

Many microwave and millimeter-wave circuits using micro electro mechanical system (MEMS) devices have demonstrated outstanding RF performance and low DC power consumption. Within regards to mechanic actuation, the majority of proposed RF-MEMS are digitally actuated devices. The fabrication of analog adjustable components like Distributed MEMS Transmission Line (DMTL) phase shifters requires several equal, tunable capacitances loading a transmission line [1, 2]. Using surface technology for the fabrication of variable capacitors seems to be difficult, since the tuning ratio is limited to low numbers [3] and the mechanical characteristics of commonly used double-clamped beams strongly depend on

residual stress and Young's modulus of thin films [2]. It can be shown that differences between individual loads result in local impedance variations and cause higher reflection losses. Recent publications on analog tunable MEMS capacitors in configurations much different from switches using polycrystalline silicon have demonstrated high tuning range with very low actuation voltage [4]. Because of long signal lines made of polycrystalline silicon partly covered with gold the quality factors and the self resonance frequencies of these devices are comparably low. The focus of this work is to demonstrate the capabilities of silicon bulk technology for the fabrication of analog tunable DMTL phase shifters. In a second part of the paper an impedance matched electromagnetic signal coupler is described. The coupler connects the MEMS phase shifter to the printed circuit board non-galvanically and therefore avoids technologically challenging metallic feed-throughs used for signal connection of packaged devices [5].

II. DMTL PHASE SHIFTER IN SILICON BULK TECHNOLOGY

For the design of analog DMTL phase shifters the silicon bulk technology offers advantages compared to surface technologies. The capability of etching structures into the single crystalline silicon, in contrast to the limitation of solely depositing and structuring thin films, allows the fabrication of actually 3-dimensional structures. This enables the design of actuation mechanisms that commonly suspend all capacitive loads and therefore minimize capacitance variations between the individual elements. Further on, the

physical separation of actuation electrodes and transmission line conductors results in a high tuning ratio and provides intrinsically high isolation between DC and microwave lines [6].

The top view in Fig. 1 and the corresponding cross section in Fig. 2 show the two wafer concept of the phase shifter. Six beam springs suspend a structured movable plate forming 25 capacitive loads. In contrast to the referenced approach [2] these loads are capacitively coupled to the ground plane of a high impedance coplanar waveguide (CPW) which is situated on the bottom wafer. The coupling capacitances change with the moving bridges. As can be seen in Fig. 2 the actuation electrodes on the bottom wafer are placed in a cavity to enhance the tunability of the functional bridge gap. The CPW is suspended on a 30 μm silicon membrane to reduce dielectric loss and to achieve high unloaded impedance despite the high relative permittivity of silicon.

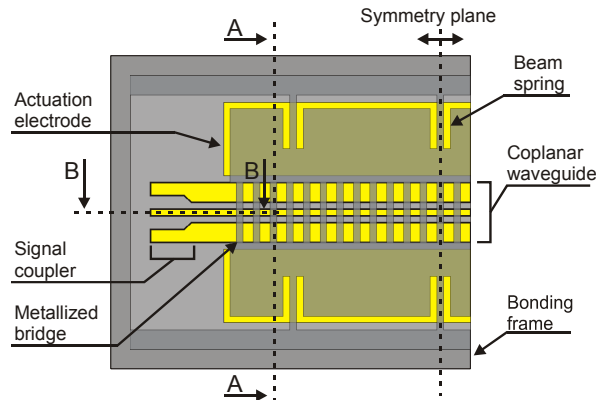


Fig. 1. Schematic top view

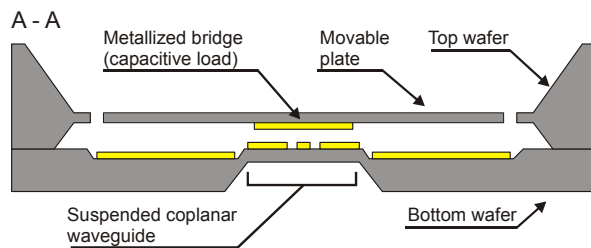


Fig. 2. Schematic cross section (cut A-A)

The tunable capacitive loading introduced by the metal bridges C_b divided by bridge spacing s

represents an additional contribution to the CPW per-unit length capacitance C_l and influences the phase velocity as well as the line impedance. The per-unit length inductance L_l remains unaffected. These assumptions are valid up to a very high upper frequency limit caused by Bragg reflections at periodic structures [2]. Following (1) the proportionality between differential phase shift $\Delta\Phi$ per line length l and frequency f evidences the true time delay characteristics of the DMTL concept. The high unloaded line impedance of the membrane suspended CPW (low C_l) results in high differential phase shift. For a higher difference in phase velocities the differential phase shift increases. Hence, the tuning ratio of the capacitive loads determines the maximum time delay. However, beside certain physical restrictions, the primary limitation results from highest acceptable VSWR caused by impedance mismatch between the phase shifter and the feed line.

$$\frac{\Delta\Phi}{2\pi f \cdot l} = \sqrt{L_l \left(C_l + \frac{C_{b,\max}}{s} \right)} - \sqrt{L_l \left(C_l + \frac{C_{b,\min}}{s} \right)} \quad (1)$$

Designing RF-MEMS devices with complex geometries requires careful considerations of component interaction. While commonly used 2.5-dimensional simulation algorithm like the Method of Moment (MoM) are good for basic design considerations, only full wave 3-dimensional simulations can provide an insight into more complex dependencies. A six-bridge subsection of the phase shifter has been implemented in a Finite Difference Time Domain (FDTD) simulator. The simulation in time domain allows the visualization of the actual wave propagation and makes analyzing of discontinuities at material boundaries possible. Fig. 3 shows exemplarily the magnitude of the electric field in between the CPW and the bridges. According to expectations, the field is concentrated between the center conductor and the metallized bridges. In consequence, the reasonable overlap length of the bridge and the ground plane is limited, since the outside of the

bridges are less penetrated by field and therefore do not provide much coupling.

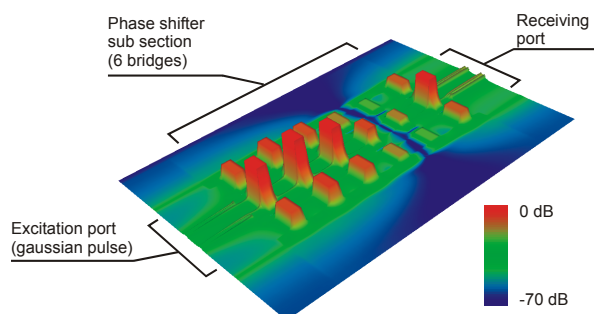


Fig. 3. Magnitude of E-field simulated by FDTD (structures set to invisible)

The design was optimized with respect to phase shift per line length. The fabricated phase shifter consists of 25 bridges with a spacing of 300 μm and a width of 100 μm . For the dimensions listed in Table 1 the FDTD and the MoM simulation predict a differential phase shift of 17°/mm line length at 24 GHz by tuning the bridge gap from 4 μm to 2 μm . This corresponds to a return loss of better than 25 dB caused by impedance mismatch. Considering metal losses and the bulk conductivity of high resistance silicon ($\rho = 3000 \Omega\text{cm}$) the simulated insertion loss of the CPW located on a 30 μm membrane is 0.8 dB/cm at 24 GHz. Due to the wide range tunability of the bridge gap the phase shift can be increased if one can tolerate more return loss. By applying the DC bias voltage of 0 - 45 V the bridge gap can be tuned from 6 - 1 μm . The actuation voltage of 45 V is chosen under the constraint that the movable plate's maximum displacement due to gravity is less than 5% of the bridge gap.

Table 1: Dimensions of the phase shifter

Bridge width	100 μm
Bridge spacing	300 μm
Tunable bridge gap	6 - 1 μm
Number of bridges	25
Center conductor width	175 μm
Ground gap	175 μm

III. COPLANAR ELECTROMAGNETIC SIGNAL COUPLER

The successful integration of RF-MEMS into microwave circuits not only depends on RF performance. For industrial acceptance, the devices need to provide high reliability and convenient handling known from their semiconductor counterparts. Many studies on MEMS have shown that hermetic sealing is important for long time stability and insensitivity against changing environmental conditions like temperature and humidity [3]. A recurring problem related to packaging is the signal connection between the microwave circuit and the insight of the die. Flip-chip bonding demands for technologically challenging through wafer vias, whereas many in-plane feed-through techniques require additional bond wires for final circuit connection [7]. In contrast to semiconductor devices, MEMS are potentially sensitive to mechanical stress. Solder connections to substrates with much different thermal expansion coefficients introduce high mechanical stress and might cause undesirable deflection and bending of the moveable structures. The electromagnetic signal coupler, shown in Fig. 4, connects the MEMS phase shifter to the printed circuit board non-galvanically using electromagnetic coupling and low stress epoxy adhesive mounting.

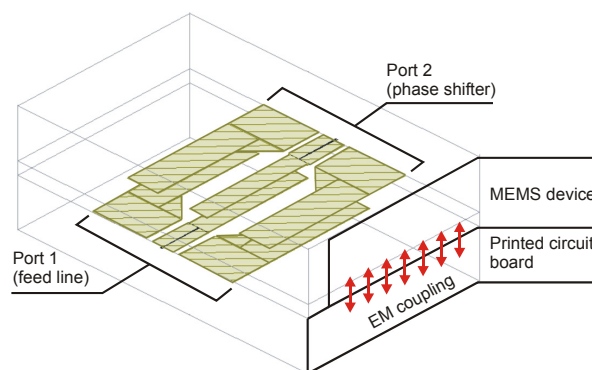


Fig. 4. Concept of coplanar electromagnetic signal coupler

Coupling between adjacent transmission lines is well known and extensively treated in many text books. A surface-to-surface transition through a chip substrate has been shown in [8]. In the case of MEMS devices the coupler needs to be integrated in a geometry mostly predefined by technology aspects. Fig. 5 shows the cross section through the chip of Fig. 1.

The section outside of the chip contains the feed line. The frame is required for wafer bonding and should provide a certain width. In contrast to the thin membrane, the solid high permittivity silicon of the bottom wafer enhances the coupling. Consequently the best position for the coupler is in between the frame and the phase shifter.

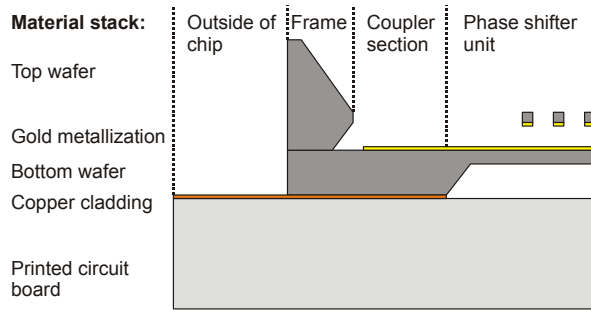


Fig. 5. Schematic cross section (cut B-B of Fig. 1)

The synthesis of couplers is often done by iterative use of analysis techniques. Conventional even- and odd-mode techniques require geometrical symmetry. The material stack according to Fig. 5 does not allow symmetry, since the printed circuit board does not have an electrically equal counterpart above the coupler. Hence, the configuration used in this design is called asymmetric and has been described by [9] using the c - and π -mode analysis technique. For setting up an analytically described model of the 2-port network the self- and mutual-capacitances C_{mn} and inductance L_{mn} have to be derived. This can be done by several ways. In ref. [10] the parameters are calculated by conformal mapping using the complete elliptic integral of the second kind. Even though conformal mapping is an exact solution, the method can not consider finite conductor thickness. Finite Element Method (FEM) simulations of a multi conductor

configuration in a 2-dimensional cross-section only provide capacitance matrices. However, performing the simulation twice, first within the given dielectric material configuration and second with the dielectric material replaced by air ($\epsilon_r = 1$), the knowledge about phase velocity in vacuum c_0 yields the missing inductance matrix according to (2) [11].

$$\begin{bmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{bmatrix} = \frac{1}{c_0^2} \begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{bmatrix}_{air}^{-1} \quad (2)$$

The derived capacitance and inductance matrices are used for the calculation of the c - and π -mode impedances and phase velocities [12] and finally for the calculation of $ABCD$ - or S -parameters [9]. In contrast to a symmetric coupler the asymmetric coupler provides different characteristics at both of its ports. This behavior can be analyzed using the concept of image impedances Z_i known from filter design. Eq. (3)-(4) [13] describe the image impedance at port one and two. The arguments of the equation are the elements of the $ABCD$ -matrix. According to the definition, the image impedance $Z_{i,1}$ represents the input impedance at port one, if port two is terminated with $Z_{i,2}$ and vice versa. Eq. (5) [13] yields an equivalent transmission coefficient γ_{eq} of the 2-port network. The primary objective of the coupler design is to find a configuration where both ports are terminated with their image impedance and where the equivalent transmission coefficient is purely imaginary. On that condition the coupler is equivalent to matched and lossless transmission line, which represents an ideal signal connection.

$$Z_{i,1} = \sqrt{AB/CD} \quad (3)$$

$$Z_{i,2} = \sqrt{BD/AC} \quad (4)$$

$$\gamma_{eq} = \cosh^{-1} \sqrt{AD} \quad (5)$$

Using the method outlined above, the coupler layout can be designed. The length of the coupling section is chosen to meet the center

frequency of 24 GHz. Comprehensive analyses have shown that under the constraint of the given dielectric material stack and meaningful conductor dimensions, there is no situation where both impedances are equal to the characteristic impedance $Z_0 = 50 \Omega$. The high permittivity of silicon and of most CPW-suited printed circuit board materials results in lower impedance values. However, choosing proper conductor dimensions, the inherent transformation ability of asymmetric couplers can be used to achieve a matched condition at port two [14]. Referring to Fig. 6, at the center frequency $Z_{i,1}$ and $Z_{i,2}$ are different. While $Z_{i,1}$ has a maximum value of much below 50Ω , $Z_{i,2}$ is matched to Z_0 . A network like this can be easily matched by a $\lambda/4$ -transformer placed in between the feed line and the coupler. With respect to Fig. 5, the high permittivity silicon entirely around the conductor below the frame allows the fabrication of low impedance lines, suitable for matching $Z_{i,1} \approx 25 \Omega$ to Z_0 .

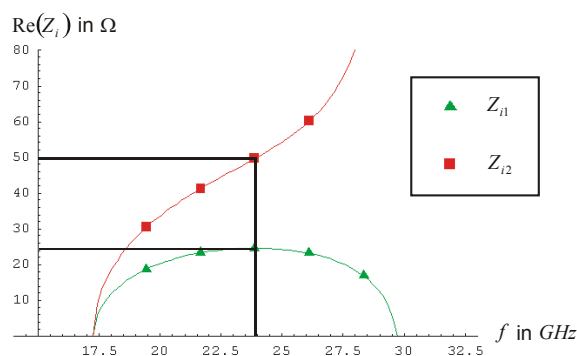


Fig. 6. Image impedances at the coupler ports

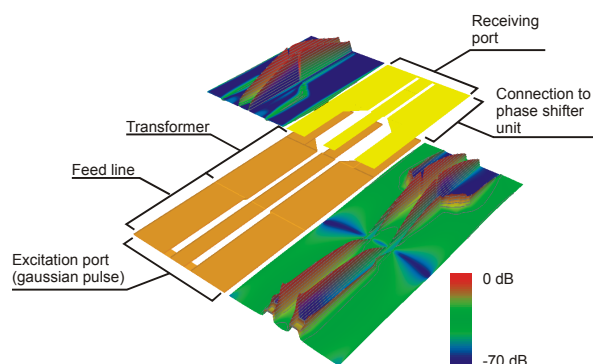


Fig. 7. Magnitude of current density simulated by FDTD (dielectric material set to invisible)

The coupler layout is optimized by full-wave FDTD and MoM simulations. The FDTD simulation results of a coupler with dimensions according to Table 2 are visualized in Fig. 7. At the center frequency of 24 GHz, the electromagnetic wave travels from the feed line on printed circuit board to the elevated CPW on silicon with a return loss of better than 20 dB and approximately 10% relative bandwidth.

The influence of possible mounting imperfectness with respect to relative displacement error has been studied by simulation as well. The coupler response is almost unaffected by relative position error of up to $\pm 50 \mu\text{m}$ in x - and y -direction. Commercially available pick-and-place automats provide less than $20 \mu\text{m}$ positioning error. Tolerances in z -direction causing an air gap between the conductor and the silicon have much stronger influence, since mode impedances and phase velocities change significantly. A possible origin of an air gap is for example the surface roughness of the copper cladding. Since simulations in the domain of surface properties are very difficult, the influence is initially neglected and then experimentally analyzed.

Table 2: Dimensions of the fabricated coupler

Strip width	150 μm
Ground gap	250 μm
Ground width	250 μm
Coupler length	850 μm
Substrate thickness (silicon)	100 μm
PCB thickness (Rogers TMM10i)	380 μm

III. FABRICATION IN SILICON BULK TECHNOLOGY

The phase shifter is fabricated in silicon bulk technology using anisotropic wet etching, reactive ion etching (RIE), silicon oxide and silicon nitride passivation and physical vapor deposition (PVD) of gold conductors. After the individual fabrication, the bottom and the top wafer are joined by silicon direct bonding.

The processing sequence of the bottom wafer is schematically shown in Fig. 8. All cavities are structured by using KOH anisotropic wet etching.

Etching in two depth levels from the backside is performed, since the desired substrate thickness of 100 μm (cp. Table 2) is too thin for wafer handling during processing. The thick frame is finally removed by dicing at the marked cutting lines. For compensation of residual stress and for isolation the conductors are deposited on 1 μm of silicon oxide. To avoid adverse conducting channels, the silicon oxide is removed between the RF conductors [10].

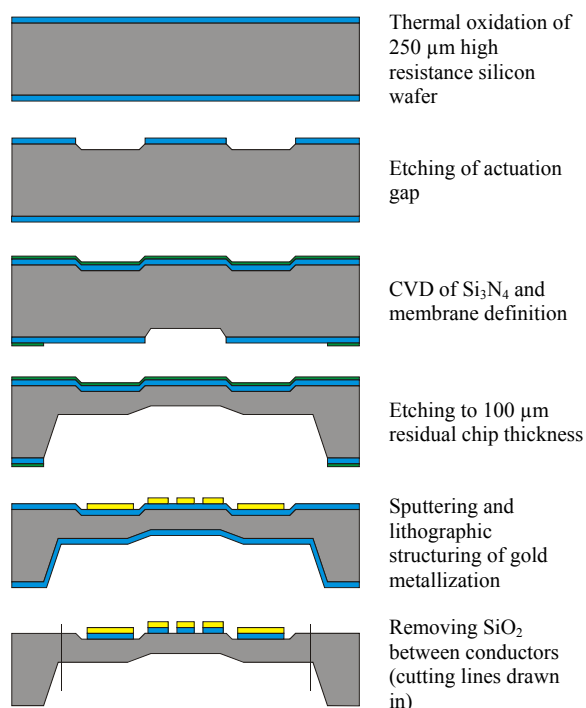


Fig. 8. Fabrication sequence of the bottom wafer

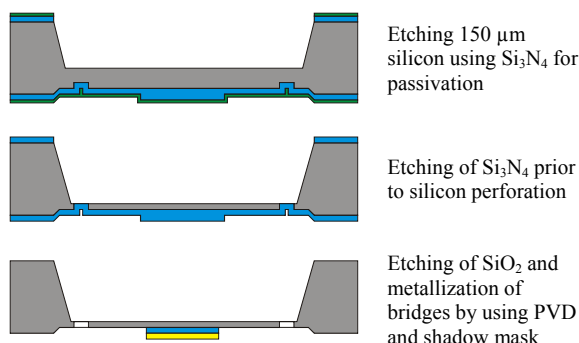
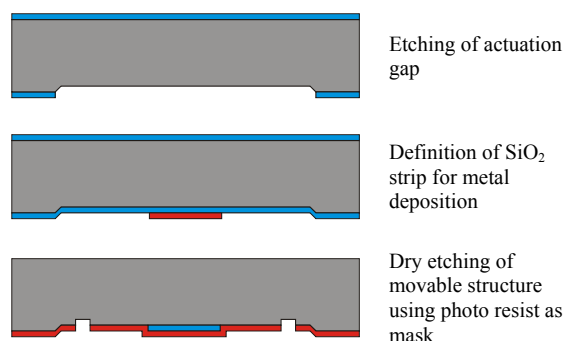


Fig. 9. Fabrication sequence of the top wafer

The process scheme of the top wafer fabrication is shown in Fig. 9. After etching the actuation gap, the movable structure is shaped by RIE and released by wet etching from the back side. The localized metallization of the bridges is achieved using PVD and a shadow mask. Fig. 10 shows a SEM micrograph of the rung-shaped metal bridges. The oxide layer underneath the metal compensates the residual stress of sputtered gold.

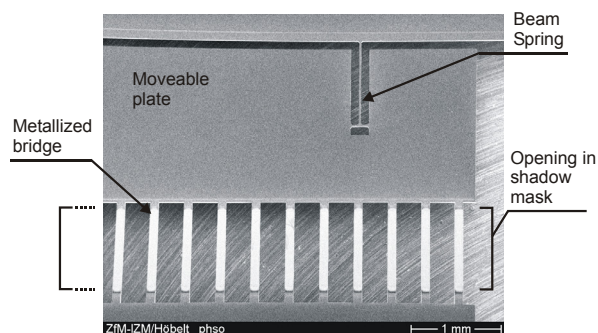


Fig. 10. SEM micrograph of the top wafer (bottom view)

Sealed packaging on wafer-scale can be achieved by bonding a cap-wafer onto the top wafer (cp. Fig. 2). This has not been realized within the first fabrication, because the accessibility with on-wafer probes was desired for separate characterization of the individual components. In contrast to surface technologies, mechanical structures fabricated in silicon bulk technology withstand bonding temperatures of at least 400°C [15] and therefore allow bonding processes like silicon direct bonding which is well-known for its excellent sealing properties.

IV. MEASUREMENT RESULTS

The fabrication of several prototype designs allows a separate characterization of the phase shifter and the signal coupler. Chips with the phase shifter, having only on-wafer probe pads, can be used to characterize the phase shifter separately from the couplers. The signal coupler is characterized with chips containing only a single coupling structure.

A. De-embedding of Device Under Test

Accurate characterization of RF components using on-wafer probes requires exact de-embedding of devices under test (DUT). Commercially available calibration standards often result in insufficient accuracy, since substrate material and conductor configuration of RF-MEMS and calibration substrates are usually different. For high accuracy, on-wafer standards have to be fabricated, assuring best possible similarity between DUT and calibration standard.

The characterization of the coupler in the setup of Fig. 11 introduces an additional challenge. Due to the nature of the signal coupler, the probe landing pads at both ports are not identical. Consequently, neither a set of on-wafer standards, nor a set of PCB-standards is suitable for de-embedding.



Fig. 11. Photograph of single coupler prototype with on-wafer probes

The Multiline Thru-Reflect-Line (TRL) procedure of the National Institute of Standards and Technology (NIST) at Boulder, CO allows using so called adapters. Adapters are 2-port networks that correct the measurements for a known error at one port. In this case, the error is

the difference between the landing pads. The sequence of calibration starts with the measurement of the on-wafer standards. The resulting calibration coefficients are applied to the measured data of the PCB-standards. Performing a new calibration using the PCB-standards priorly de-embedded with on-wafer coefficients, yield calibration coefficients that represent the difference between both sets of standards. Finally, the calibration coefficients can be converted to so-called error-boxes which represent the required adapter [16].

B. Characterization of the Phase Shifter

Fig. 12 shows the fabricated device with on-wafer probe pads for characterization of the phase shifter unit only. First available prototypes were manually bonded on chip-scale using epoxy adhesive. This resulted in a higher actuation gap and non-perfect planarity between the movable plate and the CPW. In consequence, the metallized bridges provide inhomogeneous loading resulting in impedance deviations. The prototype shows continuously tunable differential phase shift (Fig. 13) proportional to frequency, thus representing a true time delay. The measured differential phase shift for a bias voltage of 50 V is $5.4^\circ/\text{mm}$ at 24 GHz. The periodic ripples in the traces of Fig. 13 are caused by frequency dependence of imperfect impedance match. At matched condition the figure of merit is about 50° phase shift per 1dB insertion loss at 24 GHz. This is, yet, a good value compared to competing structures and principles. Nevertheless, it is expected that current investigations, in order to use silicon direct bonding on wafer-scale, yield better impedance match and significantly higher differential phase shift.

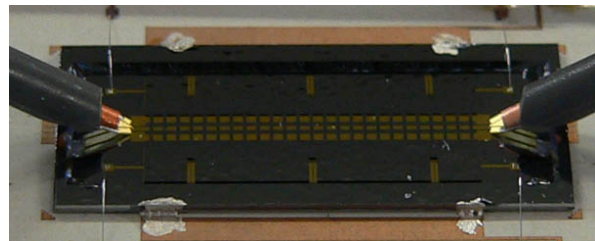


Fig. 12. Photograph of the fabricated phase shifter with on-wafer probes

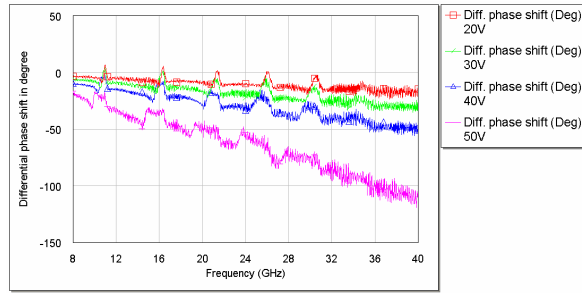


Fig. 13. Measured differential phase shift at different bias voltages

C. Characterization of the Signal Coupler

Using the de-embedding technique outlined above, the fabricated coupler shows the expected transmission behavior (Fig. 14). Due to the initially approximated effective air gap between chip and printed circuit board, the center frequency of about 28 GHz and the impedance match deviate from specifications. By comparing the measurements with modified simulation models, using different air gap heights, the air gap could be determined to be $d_{air} = 5 \mu\text{m}$. The Smith chart in Fig. 15 shows that the modified simulation matches amplitude and phase very exactly over a wide frequency band, which supports the theory that the air gap is the only reason for the observed deviations.

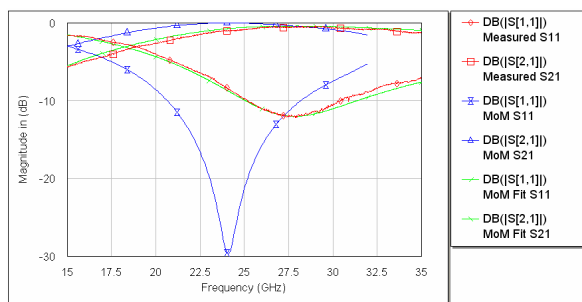


Fig. 14. Measured S -parameters of the coupler and modified simulation results approximating the air gap

Arising objectives of future work are the optimization of the mounting technique. Layout modifications with respect to coupler length and transformer dimensions are considered to result in better matching at the desired center frequency. Simulated optimizations based on the

measured numbers predict a loss per transition of 0.28 - 0.43 dB. Applying the method of normalized losses by subtracting material losses, the attenuation caused by the structure itself is expected to be 0.13 - 0.17 dB.

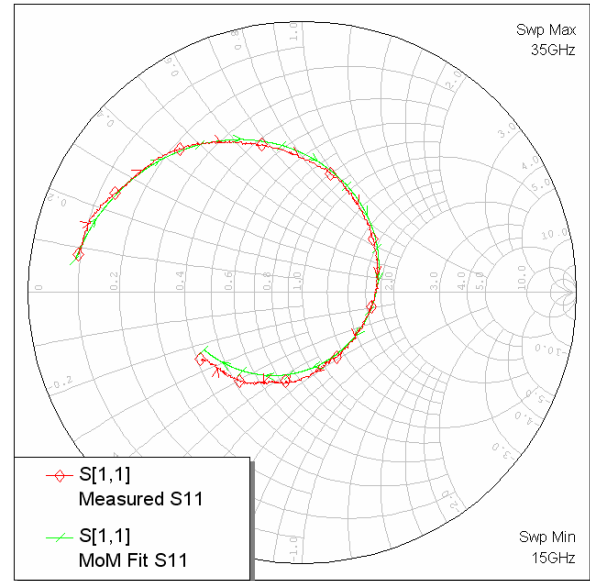


Fig. 15. Smith chart of Fig. 14 graphs

VI. CONCLUSION

A DMTL phase shifter and a coplanar electromagnetic signal coupler has been designed, fabricated, and characterized. Using silicon bulk technology enables the design of truly 3-dimensional structures and the implementation of actuation mechanisms that commonly suspends all capacitive loads on one movable plate. It is expected that the figure of merit of 50°/dB loss normalized differential phase shift can be increased by using wafer bonding. The low insertion loss and the considerably low introduced mechanical stress makes the electromagnetic coupler with epoxy adhesive mounting a promising alternative for signal connection of stress sensitive RF-MEMS.

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