INTERNATIONAL JOURNAL OF MICROWAVE AND OPTICAL TECHNOLOGY,

VOL.5, NO.6, NOVEMBER 2010

Physics based Threshold Voltage Analysis of Gate Material Engineered Trapezoidal Recessed Channel (GME-TRC) Nanoscale MOSFET and its multilayered gate architecture

Priyanka Malik[1], Rishu Chaujar[2], Mridula Gupta[1] and R.S. Gupta[1,*]

[1,*]Semiconductor Devices Research Laboratory,
Department of Electronic Science, University of Delhi, South Campus, New Delhi (India)
E-Mail: prink.malik@gmail.com, mridula_du@yahoo.com, rsgu@bol.net.in
[2]Department of Electronics, Deen Dayal Upadhyaya College, Karampura,
University of Delhi, New Delhi-110015
Tel.No.:91-11-24115580, Fax No: 91-11-24110606

***Abstract*: In this paper, a novel device structure: Multi-Layered Gate Material Engineered Trapezoidal Recessed Channel (MLGME-TRC) MOSFET has been proposed and a two-dimensional (2D) analytical threshold voltage model based on the solution of Poisson's equation in cylindrical coordinates, utilizing the cylindrical approximation, has been developed. The proposed design improves the gate leakages and increases standby power consumption to a great extent which arises due to the continued scaling of SiO2 gate dielectrics. The model accurately evaluates the channel potential, electric field, threshold voltage, drain-induced barrier lowering (DIBL), ION/IOFF ratio and sub-threshold slope. The device simulators: ATLAS and DEVEDIT have been used to verify the accuracy of the proposed model, and a good agreement between their results is obtained.**

Index Terms: ATLAS, Corner effect, DEVEDIT, GME, NJD, TRC MOSFET.

1. INTRODUCTION

During the past decade, CMOS technology has seen excellent speed and performance, achieved through improved design, the use of higher quality material; and most importantly, gate length reduction. However, scaling methodology relies heavily on the use of successively thinner gate dielectrics (≤ 3 nm) and higher levels of channel doping ($\geq 5 \times 10^{17}$ cm $^{-3}$) as feature sizes decrease in order to simultaneously achieve the desired turn-off and drive current capabilities [1, 2]. A significant consequence of aggressively down scaling the gate dielectric (silicon-dioxide, SiO_2) in MOS transistor results in direct tunneling of carriers between the gate electrode and silicon (Si) substrate [3, 4], and thus the gate and channel regions are no longer isolated from each other. This large direct tunneling current increases power consumption and degrades device performance making SiO_2 gate dielectric an undesirable material in this thickness regime [4]. Therefore, there has been much interest in finding a high-permittivity (high-k) gate insulator with greater physical thicknesses to prevent direct gate tunneling. But, the use of high-k gate material may result in dielectric thicknesses comparable to the device gate length, resulting in increased fringing fields from the gate to the source drain regions and compromised short channel performance. Thus, an ultra thin SiO_2 interlayer between the high-K layer and silicon substrate was introduced (resulting in a multi-layer gate structure) to improve the interface quality and stability. The CMOS transistors designed with multi-layer high-K gate dielectrics achieve the expected high drive current performance and lower leakage current, thereby proving its efficacy for high performance CMOS logic applications. Also, with the reduction of channel length, device encountered with

various short channel effects (SCEs) and HCEs. To achieve higher speed and current driving efficiency; and lower SCEs and HCEs, Gate material Engineering (GME) architecture (5-7) incorporation with Recessed Channel (RC) MOSFET (8, 9) can be considered as a potential candidate to suppresses and overcome the punch through and DIBL and thus proving its efficacy for high speed ULSI circuits. Thus, MLGME-TRC MOSFET considered in this study integrates the desired features of multi-layered and gate material architecture, such as improvement in gate controllability and reduction in gate leakage, tunneling effects, SCEs and improvement in carrier transport efficiency; and those allied with RC MOSFET such as excellent hot carrier immunity, SCE and punchthrough suppression, thereby enhancing the gate controllability over the channel and the electrical and switching characteristics in terms of DIBL, subthreshold swing and hot carrier effects. In order to gain an insight into the effectiveness of proposed design, the analysis takes into account the structural parameters (θ,L_p) [10], negative junction depth (NJD) and substrate doping (N_A).

II. ANALYTICAL MODEL FOR SURFACE POTENTIAL AND ELECTRIC FIELD

(a) Surface potential analysis:

In the present analysis, the channel region is divided into two parts, since the gate is made up of two different materials laterally merged together. Assuming the concave corner to be part of a cylinder, having radius $r_o = \dfrac{L_p}{2\left(1+\tan\theta_{o1}/2\right)}$ [11], Poisson equation in cylindrical coordinates for potential, i.e. $\psi(r,\theta)$, is given by

$$\frac{\partial^2\psi(r,\theta)}{\partial r^2} + \frac{1}{r}\frac{\partial\psi(r,\theta)}{\partial r} + \frac{1}{r^2}\frac{\partial^2\psi(r,\theta)}{\partial\theta^2} = \frac{qN_A}{\varepsilon_{Si}} \tag{1}$$

The potential profile in the radial direction can be approximated by a parabolic function [12] and the channel region has been divided in to two parts; hence the potential under the gate region M1 and M2 can be represented as

$$\psi_1(r,\theta) = A_{01}(\theta) + A_{11}(\theta)r + A_{21}(\theta)r^2$$
$$for \quad 0 \langle \theta \langle \theta_{01} \quad ; \quad r_o + EOT \langle r \langle r_o + EOT + y_d \tag{2}$$

$$\psi_2(r,\theta) = A_{02}(\theta) + A_{12}(\theta)r + A_{22}(\theta)r^2$$
$$for \quad \theta_{01} \langle \theta \langle \theta_{01}+\theta_{02} \quad ; \quad r_o + EOT \langle r \langle r_o + EOT + y_d \tag{3}$$

Where, EOT is the effective oxide thickness and y_d is the depletion layer thickness, given by: $EOT = t_{ox1} + \dfrac{\varepsilon_{ox1}}{\varepsilon_{ox2}} t_{ox2}$, $y_d = \sqrt{\dfrac{2\varepsilon_{Si}}{qN_A}1.5\phi_F}$

Based on boundary conditions, as shown in Fig.1 the Poisson's equation is solved separately under the two gate regions (M1 and M2) and the coefficients in (2) and (3) can be calculated as:

$$A_{oj}(\theta) = V_{SUB} - \frac{1}{\gamma}\left(\frac{1}{r_o\ln(1+EOT/r_o)}\right). \frac{(r_o+EOT+y_d)^2}{2y_d}\left(V_{gj}-\psi_{Sj}(\theta)\right) \tag{4a}$$

$$A_{1j}(\theta) = \frac{1}{\gamma}\left(\frac{1}{r_o\ln(1+EOT/r_o)}\right). \frac{(r_o+EOT+y_d)}{y_d}.\left(V_{gj}-\psi_{Sj}(\theta)\right) \tag{4b}$$

$$A_{2j}(\theta) = -\frac{1}{2y_d}.\frac{1}{\gamma}\left(\frac{1}{r_o\ln(1+EOT/r_o)}\right). \left(V_{gj}-\psi_{Sj}(\theta)\right) \tag{4c}$$

where, j =1,2 for regions under M1 and M2 respectively.

Using these coefficients, potential can be obtained as;

$$\psi_j(r,\theta) = V_{SUB} + \frac{1}{\gamma}\left(\frac{1}{r_o\ln(1+EOT/r_o)}\right).\left(V_{gj}-\psi_{Sj}(\theta)\right). \left[-\frac{(r_o+EOT+y_d)^2}{2y_d} + \frac{(r_o+EOT+x_d)^2}{y_d}r - \frac{1}{2y_d}r^2\right] \tag{5}$$

INTERNATIONAL JOURNAL OF MICROWAVE AND OPTICAL TECHNOLOGY,

VOL.5, NO.6, NOVEMBER 2010

Using this potential, Poisson equation can be solved at the surface of the channel, $r = r_o + EOT$,

$$\psi_j(r = r_o + EOT, \theta) = \psi_{Sj}(\theta) \quad (6)$$

$$\frac{\partial^2 \psi_{Sj}}{\partial \theta^2} + \frac{1}{\lambda^2}\left(\begin{array}{l} V_{gj} - \psi_{Sj}(r_o + EOT, \theta) - \\ \dfrac{1}{\dfrac{1}{\gamma}\left(\dfrac{1}{r_o \ln(1 + EOT/r_o)}\right)} \cdot \dfrac{(r_o + EOT)y_d}{(y_d - r_o - EOT)} \dfrac{qN_A}{\varepsilon_{Si}} \end{array} \right) = 0 \quad (7)$$

$$\text{Where, } \frac{1}{\lambda^2} = \frac{2(r_o + EOT)(y_d - r_o - EOT)}{y_d^2} \quad (8)$$

Introducing a new variable

$$\delta_j(\theta) = \psi_{Sj}(r_o + EOT, \theta) - V_{gj} + \frac{1}{\dfrac{1}{\gamma}\left(\dfrac{1}{r_o \ln(1 + EOT/r_o)}\right)} \cdot \frac{(r_o + EOT)y_d}{(y_d - r_o - EOT)} \frac{qN_A}{\varepsilon_{Si}} \quad (9)$$

Therefore,

$$\psi_{Sj}(\theta) = \left[\begin{array}{l} V_{gj} - \dfrac{1}{\dfrac{1}{\gamma}\left(\dfrac{1}{r_o \ln(1 + EOT/r_o)}\right)} \cdot \\ \dfrac{(r_o + EOT)y_d}{(y_d - r_o - EOT)} \dfrac{qN_A}{\varepsilon_{Si}} \end{array} \right] + \delta_j(\theta) \quad (10)$$

and substituting (9) in (17), Poisson equation reduces to a second order differential equation in $\delta_j(\theta)$ i.e. $\dfrac{d^2\delta_j(\theta)}{d\theta^2} - \dfrac{\delta_j(\theta)}{\lambda^2} = 0$ (11)

On solving differential equation in (11), we get

$$\delta_j(\theta) = \frac{\delta_{j1}(\theta)\sinh\left\{\left(\sum_{m=1}^{j}\theta_{om} - \theta\right)\Big/\lambda\right\} + \delta_{j2}(\theta)\sinh\left\{\left(\theta + \theta_{0j} - \sum_{m=1}^{j}\theta_{om}\right)\Big/\lambda\right\}}{\sinh(\theta_{oj}/\lambda)} \quad (12)$$

Using (9), $\delta_j(\theta = 0) = \delta_{11}$, $\delta_j(\theta = \theta_{o1} + \theta_{o2}) = \delta_{22}$

and boundary condition we get,

$$\delta_{11} = V_{bi} - V_{g1} + \frac{1}{\dfrac{1}{\gamma}\left(\dfrac{1}{r_o \ln(1 + EOT/r_o)}\right)} \cdot \frac{(r_o + EOT)y_d}{(y_d - r_o - EOT)} \frac{qN_A}{\varepsilon_{Si}} \quad (13)$$

$$\delta_{22} = \delta_{11} + V_{ds} - (V_{FB1} - V_{FB2}) \quad (14)$$

Using boundary conditions, as shown in Fig.1, and equations (10), (11), (12) and (13), we can obtained the value of δ_{12} and δ_{21} as

$$\delta_{21} = \frac{\delta_{11}\sinh(\theta_{o2}/\lambda) + \delta_{22}\sinh(\theta_{o1}/\lambda) + (V_{g1} - V_{g2})K_1}{K_1 + K_2} \quad (15)$$

$$\delta_{12} = \frac{\delta_{11}\sinh(\theta_{o2}/\lambda) + \delta_{22}\sinh(\theta_{o1}/\lambda) + (V_{g2} - V_{g1})K_2}{K_1 + K_2} \quad (16)$$

where $K_1 = \cosh(\theta_{01}/\lambda)\sinh(\theta_{02}/\lambda)$ and

$$K_2 = \cosh(\theta_{02}/\lambda)\sinh(\theta_{01}/\lambda) \quad (17)$$

(b) Electric Field analysis

The electron velocity through the channel is related to the electric field pattern along the channel. Thus, the electric field is given as

$$E_{Sj}(\theta) = -\frac{d}{r.d\theta}\psi_j(r,\theta)\Big|_{r=r_o+EOT} = -\frac{d}{r.d\theta}\psi_{Sj}(\theta) \quad (18)$$

where, $r = r_o + EOT$

Electric field component, under M1 is given as

$$E_{S1}(\theta) = \frac{1}{r.\lambda \sinh(\theta_{o1}/\lambda)} \begin{Bmatrix} \delta_{11}\cosh\left((\theta_{o1}-\theta)/\lambda\right) \\ -\delta_{12}\cosh(\theta/\lambda) \end{Bmatrix} \quad (19)$$

Electric field component, under M2 is given as

$$E_{S2}(\theta) = \frac{1}{r.\lambda \sinh(\theta_{o2}/\lambda)} \begin{Bmatrix} \delta_{21}\cosh\left((\theta_{o1}+\theta_{o2}-\theta)/\lambda\right) \\ -\delta_{22}\cosh((\theta-\theta_{o1})/\lambda) \end{Bmatrix} \quad (20)$$

III. THRESHOLD VOLTAGE MODEL

In GME-TRC MOSFET, due to existence of metal gates, M1 and M2, with different work functions, the surface potential minima are determined by region under M1. Thus, substituting $\psi_{S1}(r_o + EOT, \theta_{\min}) = 2\phi_F$ and $V_{gs} = V_{th}$ in the expression for surface potential under M1, we can obtain an expression for threshold voltage. The position of minimum surface potential $\theta_{\min}$ lies under the first metal gate M1 and can be evaluated as

$$\frac{\partial \psi_{S1}(r_o + EOT, \theta)}{\partial \theta}\bigg|_{\theta=\theta_{\min}} = 0 \quad (21)$$

and the minimum surface potential is

$$\psi_{S1}(\theta_{\min}) = V_{g1} - \frac{1}{M}\frac{(r_o + EOT)y_d}{(y_d - r_o - EOT)}\frac{qN_A}{\varepsilon_{Si}} + \frac{\delta_{11}\sinh\left(\frac{\theta_{o1}-\theta_{\min}}{\lambda}\right) + \delta_{12}\sinh\left(\frac{\theta_{\min}}{\lambda}\right)}{\sinh\left(\frac{\theta_{\min}}{\lambda}\right)} \quad (22)$$

Using above equation, the threshold voltage is given as

$$V_{th} = 2\phi_F + \frac{1}{M}\frac{(r_o + EOT)y_d}{(y_d - r_o - EOT)}\frac{qN_A}{\varepsilon_{Si}} - 2\exp\left(\frac{-\theta_{01}}{2\lambda}\right)\sqrt{\delta_{11}\delta_{12}} \quad (23)$$

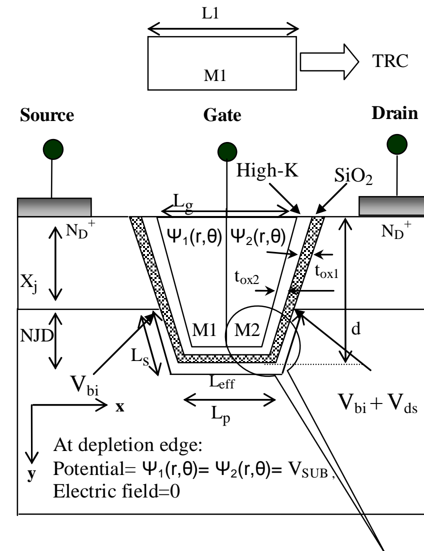
IV. SUB-THRESHOLD SLOPE

In the sub-threshold regime, as the drain voltage increases, the gate slowly loses its control over the channel; as a result, the electron concentration is not only controlled by the gate bias, but also by the nearness of the source and drain depletion regions. Thus, for a device to have a good turn-on or switching characteristics, this device characteristic should be as small as possible and can be expressed in terms of minimum surface potential and is given as

$$S = \frac{kT}{q}\ln(10)\frac{1}{\partial \psi_{S1}(r_o + EOT, \theta_{\min})/\partial V_{gs}} \quad (24)$$

where, k is boltzmann's constant and T is room temperature (300K)

6. Results and Discussion



INTERNATIONAL JOURNAL OF MICROWAVE AND OPTICAL TECHNOLOGY,

VOL.5, NO.6, NOVEMBER 2010

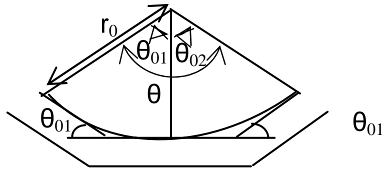


Fig.1.Schematic structure of MLGME-TRC MOSFET, where channel length $L_g = L_1 + L_2$ =74nm, with work function Φ_{M1}=4.77V and Φ_{M2} = 4.10V for MLGME-TRC and GME-TRC MOSFET and for TRC MOSFET, channel length $L_g=L_1$=74nm and work function Φ_{M1}=4.77V having Negative junction depth (NJD)=10nm, Groove Depth d=20nm, N_A =1x10^{17} cm^{-3}, N_D=1x10^{20} cm^{-3} , t_{ox1}= t_{ox2} =2nm, L_{eff}=(2 x L_s) + L_p,where L_p=28nm, L_s=14nm unless stated otherwise.

The schematic structure of MLGME-TRC, GME-TRC and TRC MOSFETs are shown in Fig.1. with metal gates, M1 and M2 of lengths L1 and L2 respectively. In MLGME-TRC MOSFET, the gate consists of multi-layered-gate dielectrics having a thickness t_{ox1} and t_{ox2} of the lower and the upper gate dielectrics, with the corresponding permittivites, ε_{ox1} and ε_{ox2}, respectively; and for GME-TRC and TRC MOSFETs: $t_{ox1} = t_{ox2}$.

Fig.2 reveals that, TRC-MOSFET with GME architecture improves the device performance with the use of two metal gates i.e. M1(control gate) and M2 (screening gate) where $\Phi_{M1} > \Phi_{M2}$, in terms of improved gate control and driving current capabilities. This is due to the step in surface potential at the interface of two metals, as shown in Fig.2, which results in screening of channel region under metal gate M1 from drain potential variations. This step in potential forces the electric field to be redistributed on the drain side. This electric field discontinuity at the interface of the two gate metals causes the overall channel field to be more uniform across the channel, as shown in Fig.3(a), resulting in the enhancement of carrier transport efficiency across the channel and hence, improves the short channel effects (SCEs), in terms of threshold voltage roll-off and DIBL, as shown in fig.4 and Table.1. Moreover, in GME-TRC MOSFET, due to the step in potential profile, the barrier height seen by the electrons at drain end of the gate is lower as compared to TRC MOSFET, leading to increased number of electrons tunneling from the channel, resulting in more sewer gate leakage current tending to increase sub-threshold slope for GME-TRC MOSFET as compared to TRC MOSFET, as evident from Table.1. Further, there is a significant improvement in I_{ON}/I_{OFF} ratio for GME-TRC MOSFET in comparison with TRC MOSFET, resulting in enhancement of switching characteristics of the proposed design. This performance enhancement in GME-TRC MOSFET is mainly because of the increased gate control and reduced SCEs.

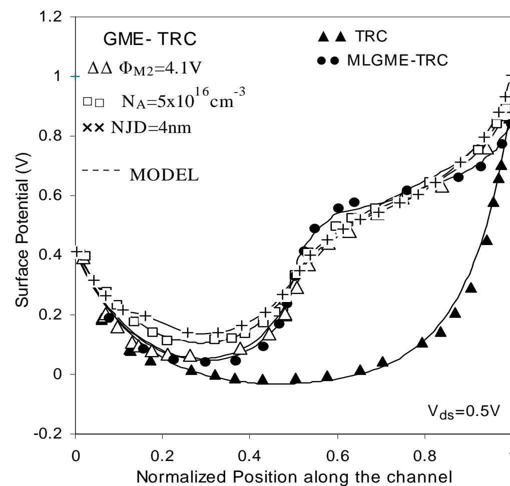


Fig.2. Potential profile for ML-GME-TRC, GME-TRC and TRC MOSFETs for different structural parameters

Fig.2. clearly depicts that for MLGME-TRC MOSFET, there is a significant enhancement in

INTERNATIONAL JOURNAL OF MICROWAVE AND OPTICAL TECHNOLOGY,

VOL.5, NO.6, NOVEMBER 2010

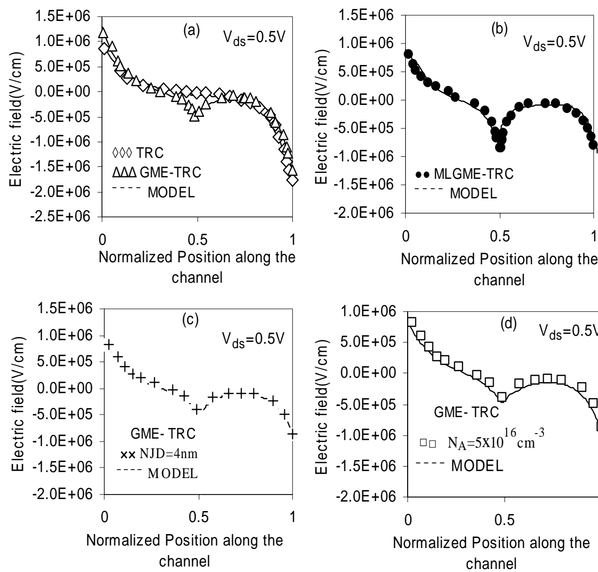


Fig.3 electric field profile for ML-GME-TRC, GME-TRC and TRC MOSFETs for different structural parameters

step in potential leading to the better screening of metal gate M1, as a consequence of the incorporation of multi-layered high-K dielectric system that facilitates physically thicker gates, thereby permitting the scaling of gate oxide thickness and thus, increasing gate control over the channel. This results in enhancement of electric field at the interface, and reduction at the drain end, as shown in Fig.3(b), thereby, improving the current driving capabilities across the channel and hence, improves the threshold voltage roll-off and DIBL, as shown in Fig.4 and Table.1, due to the improved gate control and hot carrier immunity for MLGME-TRC MOSFET. Moreover, the amalgamation of multi-layered architecture on GME-TRC MOSFET also improves the sub-threshold slope and I_{ON}/I_{OFF} ratio, as reported in Table.1 and Fig.5.

Fig.2 also reflects that, as NJD increases magnitude of minimum surface potential decreases, leading to reduced gate controllability on the channel. As NJD increases, the peak electric field at the drain end reduces, as shown in Fig.3(a and c), due to better screening of the channel from drain bias variation and improved carrier mobility, respectively; which reflect device reliability in terms of HCEs and SCEs.

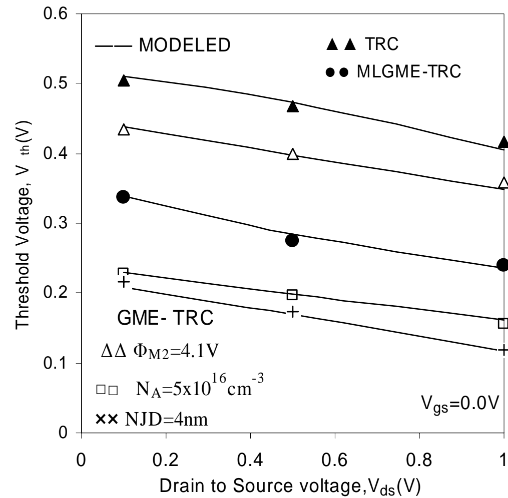


Fig.4. Threshol voltage variation for ML-GME-TRC, GME-TRC and TRC MOSFETs for different structural parameters

Further, higher NJD results in increased barriers height at corners, leading to reduced carrier velocity. Due to this, carriers require more energy to surmount these barriers, thereby raising the threshold voltage and DIBL as is evident from Fig.4 and Table.1, respectively. Higher NJDs, however, provide better switching due to reduced sub-threshold swing and better I_{ON}/I_{OFF} ratio, as is evident from the Table.1 and Fig.5, respectively. A trade-off can, thus, be made depending upon the design requirements whether the threshold voltage is the need of the design or is it the switching behavior.

IJMOT

INTERNATIONAL JOURNAL OF MICROWAVE AND OPTICAL TECHNOLOGY,

VOL.5, NO.6, NOVEMBER 2010

Parameters		DIBL	Sub-threshold slope, S (mV/dec.)
ML-GMETRC t_{ox1}=3.9, t_{ox2}=20		0.071	85
TRC		0.141	80
GME-TRC	ϕ_{M1}=4.77V, ϕ_{M2}=4.1V	0.0891	115
	NJD=4nm	0.107	150
	$N_A=5x10^{16}cm^{-3}$	0.079	153

Table.1. DIBL and sub-threshold voltage slope variation for ML-GME-TRC, GME-TRC and TRC MOSFETs for different structural parameters.

Moreover, as substrate doping decreases, the magnitude of minimum surface potential increases and electric field at the drain end decreases, as shown in Fig.2 and 3 (a and d), leading to the better gate controllability across the channel and reduced HCEs and threshold voltage and DIBL, as indicated in Fig.4 and Table.1, owing to the improved mobility across the channel. Figure clearly predicts that higher substrate doping results in higher threshold voltage, lesser sub-threshold slope, as indicated from the Fig.4 and Table.1. Thus, higher substrate doping is beneficial for better device switching speed, i.e. from OFF state to ON state, as shown in Fig.5.

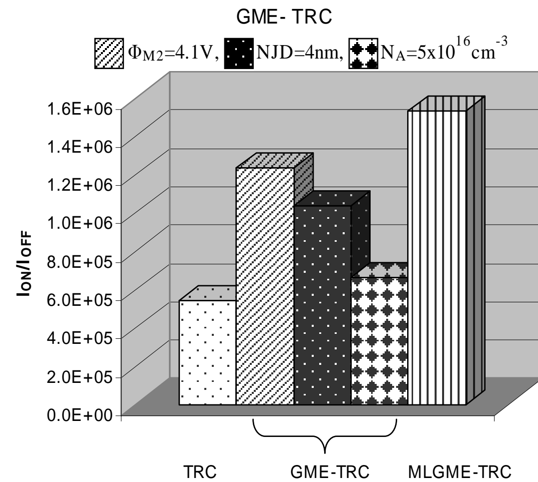


Fig.5. I_{ON}/I_{OFF} ratio for ML-GME-TRC, GME-TRC and TRC MOSFETs for different structural parameters

CONCLUSION

In this work, a novel structure, MLGME-TRC MOSFET has been proposed, analyzed and investigated using device simulators: ATLAS and DEVEDIT. The analytical and simulation results reveal that MLGME-TRC MOSFET proves to be superior to GME-TRC and TRC MOSFETs in terms of reduced DIBL, threshold voltage roll-off and HCEs; and enhanced carrier transport efficiency and switching speed of the device in terms of I_{ON}/I_{OFF} ratio. The tuning of GME-TRC structure in terms of various structural parameters has also been done and compared with MLGME-TRC MOSFET. Moreover, study shows that the sub-threshold slope increases in case of GME-TRC MOSFET due to the increased gate leakage current. However, this degradation can be minimized by incorporation of multi-layered architecture on GME-TRC MOSFET. This results in improved switching speed of the device and hence, presenting as an attractive solution for the ongoing integrating processes in digital design technology and low standby power (LSP) applications.

INTERNATIONAL JOURNAL OF MICROWAVE AND OPTICAL TECHNOLOGY,

VOL.5, NO.6, NOVEMBER 2010

ACKNOWLEDGEMENTS

Authors are grateful to Department of Science and Technology (DST) for providing the necessary financial assistance to carry out this research work.

REFERENCES

[1] Ono M, Saito M, Yoshitomi T, Fiegna C, Ohguro T and Iwai H 1995 IEEE Trans. Electron Devices 42 1822–30
[2] Taur Y et al 1997 Proc. IEEE 85 486–504.
[3] Rana F, Tiwari S and Buchanan D A 1996 Appl. Phys. Lett. 69 1104–6.
[4] Momose H S, Ono M, Yoshitomi T, Ohguro T, Nakamura S I, Saito M and Iwai H 1996 IEEE Trans. Electron Devices 43 1233–42.

[5] A. Chaudhary, M.J. Kumar, IEEE Transnsaction On Electron Devices, 51, 1463, (2004).

[6] Priyanka Malik, Sona P. Kumar, Rishu Chaujar, Mridula Gupta and R.S.Gupta, “GATE MATERIAL ENGINEE

-

[7] Priyanka Malik, Rishu Chaujar, Mridula Gupta and R.S.Gupta,“Two-dimensional Analytical Model for Trapezoidal Recessed Channel (TRC) MOSFET using Gate Material Engineering”, ISMOT 2009.

Chin J. Semiconductors, 25, 441, (2004) (in chinese).

[8] H. Ren, Y. Hao, Solid-State Electronic, 46, 665, (2002).

[9] E. Takeda, H. Kume and S. Asia, IEEE Trans Electron Devices, 30, 681, (1983).

[10] Z. Xiao-Ju, G. Xin, W. Jun-Ping, and H. Yue, Chin. Phys. Soc, 15, 631, (1980).

[11] X.J. Zhang, H.X. Ren, Q. Feng and Y. Hao,
[12] A. Kranti, S. Haldar, and R.S. Gupta, Microelectronics Engineering, 56, 241, (2001).

.