Modelling and simulation of digital-centric RF transmitters at architectural level in SystemC/AMS

Junqing Guan†, Björn Thiel†, Niklas Zimmermann‡, Bastian Mohr‡, Stefan Heinen‡ and Renato Negra†

†Mixed Signal CMOS Circuits, UMIC Research Centre and ‡Chair of Integrated Analog Circuits, RWTH Aachen University, 52074, Aachen, Germany
Tel.: +49-241-8027752; Fax: +49-241-8022199; E-mail: guan@umic.rwth-aachen.de

Abstract—This paper proposes a concept to model and to simulate the transmitter radio frequency (RF) frontend using SystemC and its analogue mixed-signal extension SystemC-AMS. The digital transmitter blocks are modeled using SystemC, while the analogue mixed-signal blocks are modeled using SystemC-AMS. These two parts of the transmitter system can be co-simulated seamlessly. Simulation results are evaluated by parsing the trace file of SystemC simulation using functions in Matlab. Based on the co-simulation and evaluation approaches, a complete platform is established. With the help of this platform, the system level simulation of RF transmitter can be carried out without many expenses regarding engineering resource. Based upon the evaluation results, it cannot only guide us to identify a suitable architecture, but also assist us to derive the design specification of each building block. The functionality of this concept as well as the benefit of employing this platform is shown in a case study through the identification of architecture and derivation of specifications for an RF-DAC based transmitter.

Along with advances in semiconductor technology, wireless technology has been evolving from cellular networks over wireless broadband networks to wireless personal area networks. An increasing number of communication standards challenges the RF transceiver design. The integration of different wireless standards is of critical importance. However, the integration should not imply an increase on the size and power consumption of the chip. A universal RF transmitter architecture supporting multiple standards will be a prospective solution, which is known as multiband, multimode, multistandardtransmitter. As we move to the commercial wireless technology deployment of the third generation partnership project (3GPP) and long term evolution (LTE), there is a great demand for the integration of a multitude of these technologies. This scenario requests that the transceiver architectures be capable to implement these new applications in a low-voltage, low-power and low-cost manner. In recent years, several state-of-the-art RF transmitter architectures are proposed, which are summarised in Sec. II.

In recent years, chip integration of complex functionality into a single silicon has become an important issue in the electronic design. The advances in technologies have allowed the development of complex systems on a single chip. With the advent of nanometer technologies, the analogue/RF and digital baseband is being integrated on to a single die to provide a low-power and cost-effective solution [1]. Furthermore, since digital design both scales better than analogue design and can be adapted easily to new processes, there is a trend to replace and support as many analogue circuitry with complex digital blocks. The design of a complex system-on-chip (SoC) is based on successful modelling methodologies, electronic design automation (EDA) tools and reusable intellectual property (IP) libraries [2].

I. INTRODUCTION

Index Terms—LTE, Transmitter, RF Frontend, Modelling, SystemC/AMS
require appropriate modelling approaches to handle
the ever-increasing complexity to achieve seamless
and high efficient simulation. SystemC is a set of C++
classes and methods that provides a mean to describe
the structure and the behaviour of hardware/software
systems from abstract specification to register transfer
level models [3]. Due to its C++ nature, SystemC
provides a good way to facilitate a connection
from system and software engineers to hardware
designers [4]. Compared with other alternatives, such
as Matlab® Simulink® or Verilog, the obvious
advantage of SystemC is that it can co-simulate both
hardware and software. In addition, it delivers adequate
performance because of the inherent high efficiency
of C++, and the comprehensive free available C++
related resources. SystemC was standardised in
2005 as IEEE 1666™ and currently only supports
the discrete-event models of computation (MoC).
However, other MoCs are supported by SystemC-
AMS, which serves as extension to SystemC, to
support mixed discrete-continuous system modelling
and simulation [5]. Fig. 1 represents the layered
structure of SystemC and its analogue/mixed signal
(AMS) extension. Based on the existing SystemC
kernel, continuous-time SystemC-AMS MoCs are
added on top of a synchronization layer which is in
charge of the communication between the SystemC
kernel and the static scheduling or other specific
solvers, such as linear network (LN) and linear signal
flow (LSF) solvers.

![SystemC and SystemC-AMS Framework](image)

Fig. 1. SystemC-AMS modelling mechanism

In this work, the focus is on how to model the building
blocks of RF transmitters SystemC/AMS, in order
to facilitate the system level simulation and early
design space exploration. With the help of simulation
results, it can guide us to identify the suitable
architecture and derive the design specifications.
Since the transmitter frontend is modelled with
SystemC which is compatible to C++, it can be
cosimulated seamlessly with various other IP blocks
written in C++.

This paper is organized as follows. Section II presents
the state-of-the-art RF transmitter architectures with
as many digital parts being of interest. In Sec III, the
details about the design flow of Systemc/AMS mod-
elling,simulation and evaluation are described. The
complete design flow consisting of simulation and
evaluation is described . Then, a high digital centric
RF-DAC based transmitter is detailed in Sec IV. In
Sec V the simulation results and derivation of spec-
cifications for each building blocks are analysed. The
paper is concluded and summarised in Sec VI.

II. RF TRANSMITTER ARCHITECTURE

The design of feasible and reconfigurable RF
transmitters for wireless applications faces many
challenges at both architecture and circuit level.
Many factors impact the choice of transmitter
architectures, such as data rate, capability of
multiband/multistandard operation and the trade-
offs between the output power, the efficiency
and the required linearity [6]. Generally, an RF
transmitter performs modulation, upconversion and
power amplification. Due to the high integration
of CMOS digital circuits and its easy adaption to new
applications, the design of RF transmitter trends to be
digitalised.

From the transmitter point of view, the key aspects
are power efficiency and linearity. Furthermore, the
transmitted signal should be limited to the frequency
band to meet air interface specifications complying
e.g. the adjacent channel power ratio (ACPR) and
spectrum emission mask (SEM). The power amplifier
(PA) has the highest power level in the transmitter
chain, which means that its linearity and power
efficiency are critical to the overall performance of
transmitters.
High data rate modulation schemes are applied to improve the channel capacity, and usually generate signals having nonconstant envelope and high dynamic ranges, due to both phase and amplitude modulation. Therefore, high linear power amplifier should be used to avoid signal distortion and power spectrum emission to the adjacent channel. However, linearity and power efficiency in RF transmitter are conflicting requirements. Therefore, advanced solutions regarding transmitter architecture have been presented, which use switching-mode PAs to make both high data rate and power efficiency possible.

\( \Delta \Sigma \) modulator is frequently applied in the cartesian modulation to shape the quantisation noise. In the work of [7] and [8], lowpass \( \Delta \Sigma \) modulator was employed for a cartesian transmitter. Since there is only 1 bit at the output of lowpass \( \Delta \Sigma \) modulator, switching-mode PAs can be utilised to achieve high energy efficiency. The I/Q bandpass \( \Delta \Sigma \) transmitter architecture proposed in [9] presents another high-efficiency candidate. The architecture is shown in Fig. 2. In this proposed architecture, two bandpass \( \Delta \Sigma \) modulators are used instead of a single one to alleviate the bandwidth requirement.

Linear amplification with nonlinear components (LINC) or outphasing RF transmitter architectures are another linearization techniques reported in the literature [10], [11]. This enables a linear power amplifier by using nonlinear building blocks. A design proposed in [12] is shown in Fig. 3. This architecture can generally improve the power efficiency of the PA. However, it is quite challenging to use PLL for wideband phase modulation, especially for LTE signals. Furthermore, two PLLs on the same chip raise the complexity as well. Besides, it is quite time consuming to simulate a PLL, although at SystemC level. Alternatively, quadrature modulation can be used for the phase modulation in LINC transmitter architecture as well, as shown in Fig. 4. This approach can remove the challenge on PLL by using quadrature modulation for phase instead. However, 4 mixers are used in this approach, which results in the increase of complexity. At the simulation point of view, it is required to model the mismatch effect for inphase/quadrature path and leakage in mixer as well. Another architecture separating phase and outphasing modulation was proposed in [13]. In this system, the outphasing vectors are created in two steps as shown in Fig. 5. In the first step, the phase of a voltage controlled oscillator (VCO) operating at carrier frequency, is modulated by \( \theta \). Then, the outphasing angle \( \phi \) is applied by delaying or advancing the output of VCO. In this architecture, only one PLL is required instead of two.

There is also another attractive transmitter architecture for power efficiency enhancement by using amplitude/phase instead of in-phase/quadrature (IQ) modulation, and the resulting transmitter system is typically referred to as polar transmitter. Fig. 6 shows the polar RF transmitter architecture proposed in [14]. This polar \( \Delta \Sigma \) modulation (PDSM) solved the noise convolution problem and can provide robust in-band signal to noise performance with a moderate oversampling rate. In Fig. 7 a PLL based polar transmitter is shown, in which either analog PLL or all digital PLL (ADPLL) [15] can be used to provide good phase resolution. This approach has low complexity, low power consumption and is capable of modulating low data rate signals, e.g. GSM signals which has a transmission data rate of 270.833 kbps. Nonetheless, it is not suitable for wideband signals due to its long settling time [16]. Fig. 8 shows another approach using
a quadrature modulator for phase modulation. The constraints coming form settling time do not exist in this structure. However, two mixers cannot only cause gain and phase mismatches regarding I/Q paths, but also increase the hardware complexity.

Besides, a pulse-width-modulation (PWM) RF transmitter is a potential alternative as well, as shown in Fig. 9, which is implemented in [17] on an FPGA. In this architecture, amplitude information is modulated on the duty ratio of a square wave which can be followed by a switching-mode power amplifier. Based upon this, phase information can be modulated on a square wave as well, therefore it is called pulse-width/position-modulation (PWPM) RF transmitter [18].

III. SIMULATION AND EVALUATION PLATFORM

As described in Sec. II, there are several potential transmitter architectures. For each application, one most suitable architecture should be found and the specification of each block in the transmitter should also be derived. Modelling and simulation is a very useful methodology for this purpose, especially when the system is too complex to be evaluated by
formular analysis. In this Section, a flow consisting of simulation and evaluation is introduced.

The simulation and evaluation platform in this work is demonstrated in Fig. 10. There are three compiled intellectual property (IP) libraries. One is the C++ library consisting of various algorithmic routines, such as fast Fourier transform (FFT), Cordic, source coding and channel coding. One is the SystemC IP library, which contains compiled models of digital transmitter blocks, such as Gaussian minimum-shift keying (GMSK), root-raised cosine (RRC) filter, orthogonal frequency-division multiplexing (OFDM), element-select-logic (ESL), RF-DAC, baseband signals of LTE, GSM and WLAN, etc. At last, there is one SystemC-AMS IP library, which includes analogue/mixed-signal models, such as mixer, PA, voltage-controlled oscillator (VCO), phase-locked loop (PLL), etc.

The transmitter architecture is described in a C++ file, in which the used modules are instanced with specified parameters and connected with each other. This architecture file can be compiled and linked with the SystemC and SystemC-AMS IP libraries by GNU C++ compiler and linker to generate an executable file.

During the simulation, the specified signals are dumped into a value change dump (VCD) file, which can be used for the evaluation. There are no built-in functions to read VCD file. Therefore, an interface called VCD parser is written to read the VCD file and transform it to the format which can be processed further in Matlab. Several evaluation functions are implemented to get parameters, such as the power spectral density (PSD), error vector magnitude (EVM), adjacent channel power ratio (ACPR), signal-to-noise ratio (SNR), and bit error rate (BER).

It is worth mentioning that this platform can be extended easily by adding more models in the SystemC/AMS IP and C++ algorithm libraries as well as more Matlab functions for data evaluation. Various transmitter architectures can be simulated and evaluated by enriching the libraries of models and evaluation functions. With this platform, design space exploration, simulation and verification of transmitter architectures can easily be completed. In the following, several important blocks are represented in detail.

![Fig. 10. Platform for exploration of RF transmitter architecture](image)

**A. Digital Signal Generation**

In order to simulate the transmitter, baseband signals of different standards at physical layers should be provided. In Fig. 11 and 12, baseband signals of GSM, WLAN 802.11 a/g and LTE uplink are generated according to blocks. In GSM, GMSK modulation with a time-bandwidth-product (BT) of 0.3 is used. This model can be reused for Bluetooth as well by changing the value of BT to 0.5. The generation of WLAN 802.11 a/g and LTE Uplink are quite similar, since they both use OFDM for baseband modulation. The difference is that WLAN has an OFDM of 64 subcarriers, among which 52 subcarriers of 312.5 kHz are used. LTE has an OFDM of 2048 subcarriers, among which a different amount of subcarriers can be used according to the bandwidth.
The power amplifier in this work is modelled using the Saleh model [19]. Assuming the baseband signal is quadrature modulated as inphase/quadrature components,

\[ I(t) = A(t) \cos(\Phi(t)), Q(t) = A(t) \sin(\Phi(t)) \]  

(1)

and the output of power amplifier is \( y(t) \),

\[ y(t) = g[A(t)] \cdot \cos(\omega_0 \cdot t + \Phi(t)) + \phi[A(t)] \]  

(2)

the AM/AM and AM/PM distortion of Saleh model is represented with \( g[A(t)] \) and \( \phi[A(t)] \), respectively. According to the work in [19], two parameters, \( \alpha_a \) and \( \beta_a \) are used to identify the amplitude distortion. For phase distortion, two other parameters, \( \alpha_\phi \) and \( \beta_\phi \) are used as well.

\[ g(A) = \frac{\alpha_a \cdot A}{1 + \beta_a \cdot A^2} \]  

(3)

\[ \phi(A) = \frac{\alpha_\phi \cdot A^2}{1 + \beta_\phi \cdot A^2} \]  

(4)

Generally, 4 parameters are used for the configuration of PA and they are gain \( (G_v) \), 1dB compression point \( (P_{1dB}) \), phase distortion at the 1dB compression point \( (\phi_{A_{1dB}}) \) and maximal phase distortion \( (\phi_{max}) \). These 4 parameters are different to those in Saleh model. Assuming a 3rd order polynomial model is used, then 4 parameters, \( \alpha_a, \beta_a, \beta_\phi \) and \( \alpha_\phi \), are derived for the calculation of \( g(A) \) and \( \phi(A) \) in Saleh model.

\[ \alpha_a = \frac{10^{G_v/20}}{2} \]  

(5)

\[ \beta_a = \frac{1}{A^2_{1dbcp}} \]  

(6)

\[ \beta_\phi = \frac{1}{\phi_{max} - \phi_{A_{1dB}}} \cdot \frac{1}{A^2_{1dbcp}} \]  

(7)

IV. RF-DAC TRANSMITTER ARCHITECTURE

In this section, a new RF-DAC transmitter architecture is introduced and the functionality of each block is explained. Basically, the RF-DAC is a combination of a current-steering DAC and a mixer, and it was proposed at first by Luschas [20]. Since there is no filter between the DAC and mixer, it reduces the complexity of system. In order to mitigate the effects of switching distortion, the oscillating waveform should be set to be a multiple \( (k \ast f_s) \) of the sampling frequency \( f_s \).

The RF-DAC transmitter architecture proposed in [21] is shown in Fig. 13. It employs a digital intermediate frequency (IF) quadrature mixer, and a bandpass ∆Σ modulator and an RF-DAC. However, in this the direct upconversion architecture is modelled. Therefore, two RF-DACs are employed for inphase/quadrature path and there is no IF quadrature mixer anymore.

Fig. 14 shows the detailed block diagram of the RF-DAC based transmitter in this work. As shown, the digital baseband signal is generated on the left hand side. The signal can be either orthogonal frequency-division multiplexing (OFDM) signal in the case of LTE downlink, or single-carrier frequency...
division multiple access (SCFDMA) signal, in the case of LTE uplink. Each subcarrier can be modulated by different techniques, such as QAM, QPSK, GMSK, etc, and each subcarrier has a defined frequency spacing (15 kHz for LTE, 312.5 kHz for WLAN 802.x). Actually, it is very convenient to have reconfigurable parameters in SystemC. Either constructor parameters or template parameters can be used. Besides, many other IP blocks can be reused, e.g. FFT. Therefore, in the OFDM block, one does not need to program FFT on the scratch. Free and efficient FFT code can be reused, which saves us certain effort. In order to improve the immunity to multipath fading, cyclic prefix is appended at the front of each OFDM/SCFDMA symbol. Normally, LTE defines the cyclic prefix length of 4.7 us, i.e. 144 samples. In order to cover large cell scenarios, cyclic prefix can also be extended to a length of 16.7 us (512 samples).

Then, the baseband data is separated into inphase, $I$, and quadrature, $Q$, part. They are further processed for pulse-shaping by root-raised-cosinus (RRC) filter to minimise intersymbol interference (ISI) and perform matched filtering at the receiver. For the modelling of filter, specifications are given to matlab routines which derive the implementation details, e.g. the order of filter and tap coefficients. Then, SystemC models based on these parameters can be generated automatically. It facilitates us to simulate different filters and assist us to find the optimal candidate.

High bit resolution should be used in the digital circuitry to keep the quantisation noise below acceptable level. However, more bits means more area and power dissipation for the RF-DAC. Therefore, a $\Delta \Sigma$ modulator is used to reduce the bit resolution by applying noise-shaping technique to quantisation errors.

Nonlinearities in multibit current-steering DAC originate from static and dynamic mismatch and switching imperfections. Data-weighted-averaging (DWA), tree-structured (TS) and segmented mismatch shaping (MMS) techniques are introduced to avoid the nonlinearity. The element-selection-logic (ESL) block before the RF-DAC is in charge of MMS by applying DWA, TS or segmented MMS algorithms. After this, the RF-DAC is used to perform the digital-to-analogue conversion and upconversion to carrier frequency, followed by a bandpass butterworth filter. At last, a linear power amplifier (PA) is used to amplify the transmitted signal.

V. SIMULATION RESULTS

In the following, the simulation results of the RF-DAC based transmitter modelled in SystemC/AMS in Fig. 14 are represented. According to these results, some design specifications can be derived for each blocks.

<table>
<thead>
<tr>
<th>Block</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>QAM</td>
<td>rectangular 16 QAM</td>
</tr>
<tr>
<td>SC Mapping</td>
<td>distributed mapping</td>
</tr>
<tr>
<td>SCFDMA</td>
<td>subcar.(1200), ifft(2048), cp(144), roll-off(51)</td>
</tr>
</tbody>
</table>

The baseband signal settings are shown in Table 1. For the modulation of each subcarrier, 16-QAM is used. According to the LTE uplink specification, OFDM is used for modulation. Among the total 2048 carriers, 1024 subcarriers are used, so the bandwidth is about 15.36 MHz (each subcarrier has a symbol rate of 15 kHz). To create guard intervals in front of each symbol, cyclic prefix of 144 samples (4.7 us for a medium-size cell scenario) are appended. Besides a windowing of 51 samples (2.5 % of a complete symbol samples) is used to smoothen transition between symbols.

Pulse shaping is used to improve ISI. In this work, a RRC filter having a roll-off factor 0.22 and over sampling rate (OSR) of 4 is applied. The power spectrum density after the RRC filter is shown in Fig. 15, which has about 60 dB suppression at the first image.

As mentioned in Sec. II, the oscillating frequency should be multiples of the sampling frequency to reduce glitches. In this RF-DAC transmitter, the factor is set to 3. Therefore, the signal should be upscaled and filtered to around 800 MHz. Fig. 16 shows the spectrum after the interpolation filter, which consists of two FIR filter of 23rd and 20th order.
In order to have sufficient low quantisation noise, the
digital signals are processed with 14 bit resolution in
building blocks before DSM. However, this is quite
challenging for following building block, i.e. RF-
DAC, therefore ΔΣ modulator is used to reduce the
bit resolution. Noise shaping from 1st to 3rd order
ΔΣ is simulated, and the resulting output spectra are
compared in Fig. 17. As expected, the 3rd order ΔΣ
modulation gives the best performance.

Different bit resolution of the 3rd ΔΣ modulator are
simulated as well and shown in Fig. 18. With 9 bit
resolution, the quantisation noise is about 95 dB lower
than the signal at 20 MHz offset frequency.

In an RF-DAC, the static mismatches between the
current cells are inevitable. Monte Carlo simulations at
schematic level shows a static mismatch of 10 %, and
in this work we assume the mismatches are normally
distributed. In Fig. 19 several MMS approaches are compared, assuming the static mismatch $\sigma = 0.1$ and no dynamic mismatch. For the static MMS, the $1^{st}$ order TS and DWA approaches are compared, while for the dynamic MMS, the Return-to-Zero (RTZ) and no dynamic MMS are compared. As further shown in Fig. 19, the DWA MMS without dynamic MMS approach has nearly the same performance as the $1^{st}$ order TS MMS without dynamic MMS. Both have about 15 dB more suppression for mismatch noise compared to nonstatic MMS. In this simulation we assume there is no dynamic mismatch, therefore, the RTZ dynamic MMS approach even worsens the performance compared to no dynamic MMS.

In Fig. 20, besides static MMS, we also take dynamic mismatches of $\Delta \tau = 0.05$ into account. The simulation results show that, it is worth to apply the RTZ MMS for dynamic mismatches. This leads to 4 dB and 10 dB more suppression for static DWA and $1^{st}$ order TS MMS approaches, respectively. For the following simulations, the DWA and RTZ MMS approaches are used due to their simple implementations.

Based on these results, the specifications of each block are derived and summarised in Table 2. These specifications are used as parameters for each SystemC or SystemC-AMS model. In this case study, 64-QAM and 2048 OFDM modulation is applied for a symbol stream of 30.72 MS/s, followed by a RRC filter with OSR of 4, roll-off factor of 0.22 and order of 56. The last stage is a PA, which is modelled with a gain of 20 dB, $P_{1\text{dB}}$ compression point of 28 dBm, 0.1 rad phase distortion at $P_{1\text{dB}}$, and a maximal phase distortion of 1 rad. The simulated output PSD of the RF-DAC transmitter shows a suppression of out-of-band emissions of more than 60 dB, as shown in Fig. 21. The simulation of a data stream of 4 s of the equivalent baseband model is about 43.76 s on a duo CPU at 3.0 GHz and 4 GB of memory.

<table>
<thead>
<tr>
<th>Block</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>RRC</td>
<td>osr(4), roll-off(0.22), delay(7), order(56)</td>
</tr>
<tr>
<td>SDM</td>
<td>$3^{rd}$ order single loop $\Sigma\Delta$ modulator, bits(9), osr(7)</td>
</tr>
<tr>
<td>ESL</td>
<td>DWA (static MMS), RTZ (dynamic MMS)</td>
</tr>
<tr>
<td>RF-DAC</td>
<td>$\sigma = 0.1$ (stat.), $\Delta \tau = 0.05$ (dyn.)</td>
</tr>
<tr>
<td>BP</td>
<td>$2^{nd}$ order butterworth filter, quality factor $Q=10$</td>
</tr>
<tr>
<td>PA</td>
<td>gain(20 dB), $P_{1\text{dB}}$=28 dBm, $\phi_{1\text{dB}}$(0.1), $\phi_{\max}$(1)</td>
</tr>
</tbody>
</table>

![Fig. 19. Comparison of mismatch shaping approaches ($\sigma = 0.1, \Delta \tau = 0$)](image)

![Fig. 20. Comparison of mismatch shaping approaches ($\sigma = 0.1, \Delta \tau = 0.05$)](image)

![Fig. 21. Power spectral density at the output of the modelled RF-DAC transmitter](image)
VI. Conclusion

The paper describes the system level modelling approach for a selected RF transmitter architecture using SystemC and System-AMS. Digital blocks are modelled with SystemC, while analogue/RF blocks are modelled with SystemC-AMS. The concept is proven to be co-simulated seamlessly. Based on the simulation results, design specifications are derived for each block. A platform integrating modelling, simulation and evaluation is developed. This platform can be applied for exploring design specification and system verification of future digital-centric RF transmitter frontends.

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