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Multi-wafer Bonding, Stacking and Interconnecting of Integrated 3-D MEMS Micro Scanners

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***Abstract* - In this work we describe the bonding and contacting of a micro machined vertically integrated 3-D micro scanner, which is a key-component for a number of scanning imaging micro systems, such as confocal microscopes on-chip or optical coherence tomography (OCT) probes for micro endoscopy. The 3-D micro scanner is composed of two electrostatic silicon MEMS micro actuators which are vertically aligned and bonded with glass and ceramic components to create hermetically sealed cavity for scanning micro lenses. In addition, the through wafer vias (TWV) technology is employed to establish electrical connection from the top to the bottom through a stack of two SOI wafers, one glass wafer and one ceramic wafer. Presented methods are of general importance for various silicon-based vertically integrated devices.**

***Index Terms* - assembly technology, bonding, glass micro lens, MOEMS, optical micro scanner, vertical integration.**

I. INTRODUCTION

The lack of miniaturization in conventional 3-D display and imaging systems limits their application fields and imaging capabilities. Responding to strong consumer demand for ultra-compact devices and global passion for “greener”, more power-efficient products, marketplace demands are also pulling 3-D integration into the mainstream.

Firstly, micro-opto-electromechanical systems (MOEMS) technology combining MEMS and micro-optics is well suited for manipulating light. A number of different ways can be envisioned to scanning, steering, or modulating the light beams. This technology allows a large array of micromechanical light manipulators to be batch-fabricated at low cost. A number of MOEMS display and imaging products and technology demonstrators have been developed for defense, aerospace and medical markets in the form of miniature devices for projection displays, imaging devices, barcode readers, and scanners. Secondly, the use of the 3rd dimension by employing multi-wafer integration, stacking and interconnecting several functional wafers based on disparate technologies, enables the creation of truly 3-D devices that are smaller, thinner and lighter in weight than existing devices.

The main goal of this work is to design, develop and validate experimentally a fully integrated prototype of vertically integrated micro optical scanner, suitable for a wide number of imaging systems such as the confocal microscopes on-chip or OCT probes. One of the challenges of this project is the proposed 3-D packaging that combines several dies vertically by using multi-wafer technology. This approach offers the possibility to fabricate complex MOEMS device that consists of vertically stacked building blocks (micro lens in glass, Si MEMS micro actuator, beam splitter, detector) and effective integration of heterogeneous technologies in a minimum space.

This paper describes the methods of bonding of two silicon MEMS micro actuators (X-Y scanner, Z-scanner) with other glass and ceramic components of 3-D micro scanner as well as their simultaneous electrical connections by vertical through wafer technology.

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II. DESIGN AND BONDING CONCEPT

Design

The design of the 3-D micro scanner relies on vertical integration of five silicon, glass and ceramic building blocks, which are mechanically and electrically connected on the wafer level (Fig. 1). The silicon components are electrostatic X-Y and Z micro actuators, described elsewhere [1, 2]. Two glass scanning micro lenses are integrated onto movable platform of these micro actuators to provide well controlled deflection of laser beam, whereas one glass micro lens is monolithically integrated within bottom lid for focusing purposes. The integration of micro lenses is realized by glass frit bonding using a paste, which melts at relative low temperature (420°C).

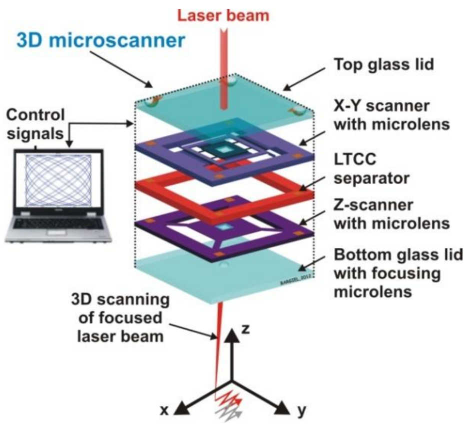

Fig. 1: Conceptual drawing of the vertically integrated 3-D micro scanner

Glass substrates encapsulate also the whole device from both sides while ensuring the optical transparency through the stack. Due to optical reasons, the distance between scanning micro lenses has to be well controlled within tolerances of a few micrometers. This is achieved by use of mechanical spacer made of low temperature co-fired ceramic (LTCC), which can be anodically bonded to silicon due to matched coefficient of thermal expansion. In order to drive electrostatic micro actuators, sandwiched between glass and ceramic components, the technology of through wafer vias (TWV) is applied to create electrical connections from the pads, located on the top glass lid, through the stack of two SOI wafers, one glass wafer and one ceramic wafer. The cross-sectional view of individual chip is presented in Fig. 2. The vias on different levels of the stack are connected during sequential multi-level anodic bonding forming pressure-contacts between Cr/Au pads.

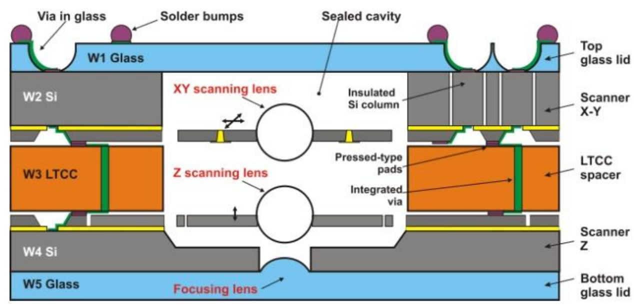

Fig. 2: Cross-sectional view of 3-D micro scanner

Bonding concept with technology results

In order to assemble the whole MEMS scanner seven different substrates have to be bonded. Based on this stack three different bonding technologies are necessary. These are Si-Si direct bonding to fabricate the customized SOI substrates for scanner etching, the glass-Si anodic bonding to protect the scanner against the environment and the LTCC-Si bonding to mechanically and electrically join the X-Y scanner with the Z scanner. Furthermore the LTCC has the task to create the space between both scanners to allow free movement of the micro lenses. Because the anodic bonding can only be realized between Si and glass or Si and LTCC, respectively the bonding sequence has been chosen in way that Si and glass or LTCC are used alternatively to each other. The bonding sequence starts with fabrication of SOI wafer including the etching of a cavity near 80µm depth into a Si-basic wafer shown in
Fig. 3.

Afterwards a direct bonding process against a SOI wafer with a device thickness of 15µm (buried oxide thickness 0.5µm, 400 µm handle

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wafer thickness) takes place. The quality of the bonding step is recorded by infrared microscope. Fig. 4 shows the results of this bonding step. The IR-transmission shows few, small defects (voids) located at the wafer edge within a 0.5 cm exclusion zone.

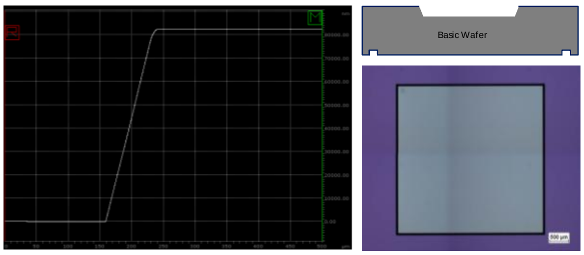

Fig. 3: Fabrication of Si-basic Wafer for Z-scanner; Left: profile measurement; right: light microscope image, cross section and top view

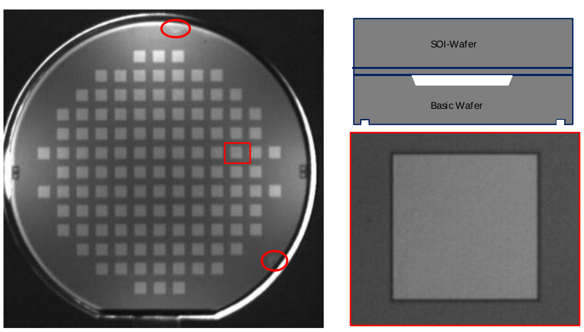

Fig. 4: IR-transmission of the bonding interface; Left: IR-transmission of whole wafer; Right: IR-transmission of single chip

For this direct bonding a wet pretreatment, a vacuum bonding process and an annealing step are applied. The pretreatment consist of RCA1, RCA2 and again RCA1. The bonding is done at low pressure (<1x10-4 mbar) using a standard bonding equipment. For the annealing step the parameters are 800°C, 6h in nitrogen in a horizontal furnace. Next step is the thinning of the handle wafer up to the stop of the buried oxide. The fabrication of large cavities (cavity size 4mm x 4mm) covered with thin membranes (thickness 15µm) requires a thinning process step based on KOH etching and edges trimming by grinding. Exemplary shows Fig. 5 left cracks directly over the cavity edge after grinding.

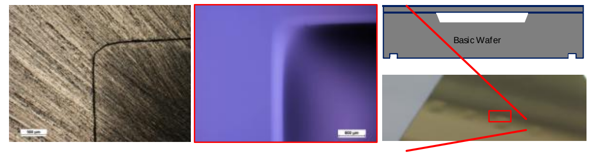

Fig. 5: Thinning of the handle-wafer with and without cracks over the cavity after thinning; Left: with cracks; Right: without cracks

These semi-finished substrates are used to etch the X-Y scanner as well as the Z scanner with the through holes etched from the backside.

At the beginning of the LTCC-Si bonding process a glass ball lens has to be integrated into the Z scanner. Next wafer 4 (Z-scanner) and wafer 3 (LTCC spacer) are bonded anodically, schematically shown in Fig. 6.

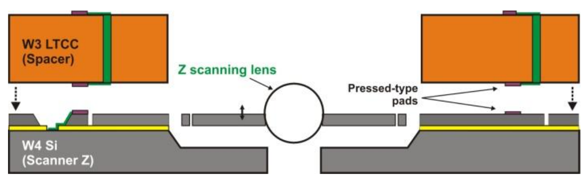

Fig. 6: Anodic bonding between wafer 4 (SOI substrate) and wafer 3 (LTCC)

This first stack must be bonded to the X-Y scanner based on an anodic bonding process also. In this case the interface consists again of LTCC and Si.

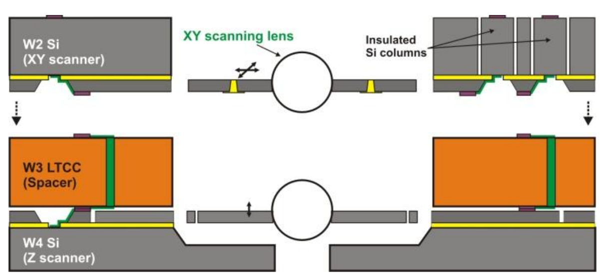

Fig. 7: Anodic bonding between first stack (wafer 4 and wafer 3) and wafer 2 (X-Y scanner)

Afterwards a second lens has to be integrated into the X-Y scanner. To close the system a cap lid has to be bonded on top. The cap lid is formed from borosilicate glass and can be anodically bonded to the scanner stack. The glass wafer contains isotropic etched holes for contacting the underlying layers.

The last step to realize a hermetic sealing a bottom lid made of glass must be bonded on the bottom side of the Z scanner. That can also be done anodically.

Because all the necessary contacts (GND, driving voltage 4x - X-Y scanner and 1x - Z scanner) should be on the top side of the top lid, vertical through silicon/glass/LTCC vias have to be integrated. During the wafer bonding the contacts on each wafer must be connected to the next level. The contacts between the wafers two, three and four are formed by gold thermo compression bonding during the anodic bonding processes of the wafers stacks. The used chromium/gold layer thickness is 10/100nm thick. The contacts in the holes in the top glass lid are sputtered directly after the wafer bonding by applying again chromium/gold 10/1000 nm thick.

This bonding concept was chosen because we have to integrate three different materials. Glass is necessary for the optical system. This is a reason why other materials are necessary which are compatible to the used glass and which give us the opportunity to form the scanners as well as the spacer. The applied LTCC material has a similar CTE to the glass and Si and is also anodically bondable. Si on the other hand is well known for the structuring of the X-Y and Z scanner. Concluding the anodic bonding, as a very simple bonding technology, is especially fitted to assemble the prefabricated components into an optical system. In addition, anodic bonding does not need additional interface materials therefore it does not increase the mechanical stress of the whole stack.

III RESULTS

Anodic Bonding Si- LTCC

LTCC is composed from glass and ceramic filler material. The CTE is determined by the particle size and particle form. The sintering temperature of this LTCC is adjusted around 800°C to 900°C, which is below the melting temperature of low resistance conductors, such as Ag and Au. These materials can be used for LTCC via filling. Cavities and interlayer connecting vias are created by pin punching the green sheet, and then the vias and conductors are screen printed, and finally laminated and fired. This is an IVH (Interstitial Via Hole) structure, which allows easy processing of the vias and unrestricted positioning of the vias. IVH also offers flexibility to the design of the internal layer patterns. **Error! Reference source not found.** is a SEM cross-section photo of a LTCC substrate sample. For the bond strength the temperature and the voltage are of great importance. Therefore we varied the temperature and the voltage to evaluate their influence on the fracture toughness. For this purpose we applied similar bonding sequence like for borosilicate glass. The temperature has been changed between 300°C and 400°C and for voltage we used two different values, 400V and 800 V, respectively. As the result we can see that the temperature has the higher influence. At 400°C the fracture toughness is comparable to borosilicate glass.

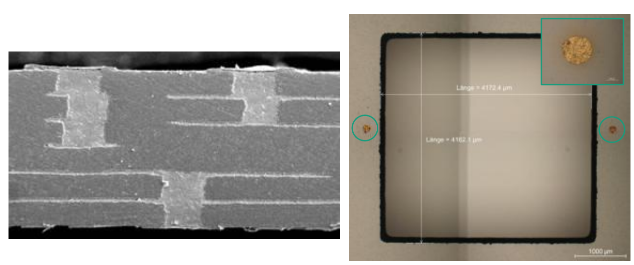

Fig. 8: SEM cross-section photo (left) of a LTCC multi-layer spacer substrate (6 layers) with integrated vias and light microscope image (right) of the fabricated LTCC-spacer (thickness 700µm and 100µm via diameter). [3]

With decreasing temperature the fracture toughness decreases faster than during the Si-glass bonding (see

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Fig. 9). For the application fracture toughness higher than 0.6 MPa√m is acceptable. From experimental results can be concluded that at bonding conditions of 400°C and 400V this value can be achieved.

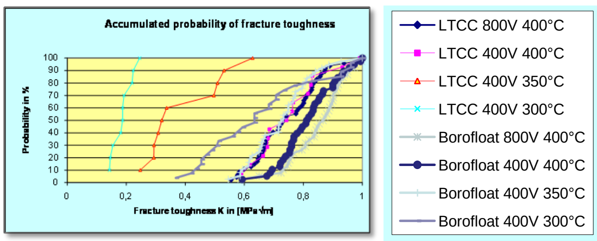

Fig. 9: Comparison of fracture toughness of LTCC/Si and Glass/Si bonds at different bonding parameters.

The bonding yield, defined by a value higher than 0.6 MPa√m, is more than 90%.

In order to prevent a short cut though the vias, integrated into the LTCC between the top electrode and the Si substrate, an additional glass spacer between the LTCC and the top electrode is used during the bonding process. The electrical contact formation between the gold layers on both substrates can be realized in parallel with the described bonding process. Designing a contact area of 100µm x 100µm a contact resistance smaller than 3.5 ohm could be realized.

Thermo compression bonding of gold contacts

The contacts between the wafers W2 and W4 and the ceramic wafer W3 are formed by gold thermo compression bonding during the anodic bonding processes. The used chromium/gold layer thickness is 20/200nm thick, deposited by sputtering. Pre tests for gold/gold contact formation have shown that a temperature of at least 300°C are necessary to form a low ohmic contact. The thermo compression bonding was done in a SUSS wafer bonder at 400°C for 30 minutes at a tool pressure of 7 MPa. Before annealing we measured the electrical resistance between both wafers (middle wafer and top or bottom counter wafer) showing values between 2 and 4.8 ohm with a mean value of 3.5 ohm having a contact area of 100µm x100µm. After an annealing step at 300°C for 3h the contact resistance decreased to a mean value of 3.2 ohm (see
Fig. 10).

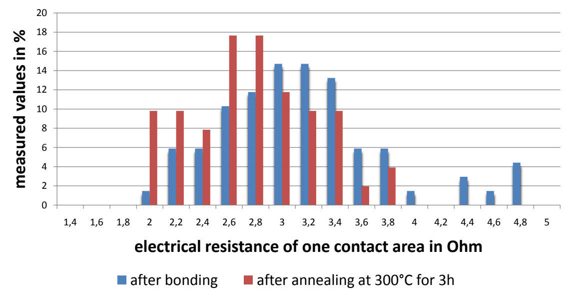

Fig. 10: Contact resistance measurements after gold/gold thermo compression bonding

The reliability of the contacts has been tested by thermal shock cycles (100 cycles, -40°C to 120°C, 30min-1min- 30min). To compare the results we measured the pull strength before and after shock loading. The results have shown that the shock loading has no significant influence to the fracture force (see
Fig. 11).

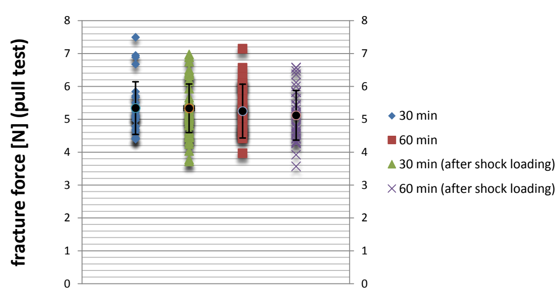

Fig. 11: Distribution of fracture force (pull test) before and after shock loading in dependence of bonding time (30 min and 60 min)

The results show that there is no obvious impact of bond time and shock loading to the fracture force of the gold/gold thermo compression contact.

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