Robust GaN MMIC Chipset for T/R Module Front-End Integration

Ernesto Limiti1*, Sergio Colangeli1, Andrea Bentini1 and Walter Ciccognani1

1Dipartimento di Ingegneria Elettronica, Università degli Studi di Roma Tor Vergata,
Via del Politecnico 1, 00133, Rome (Italy)
Tel: +39-0672597351; Fax: +39-0672597935; E-mail: limiti@ing.uniroma2.it

Abstract - In this contribution, a set of robust GaN MMIC T/R switches and low-noise amplifiers, all based on the same GaN process, is presented. The target operating bandwidths are the X-band and the 2-18 GHz bandwidth. Several robustness tests on the fabricated MMICs demonstrate state-of-the-art survivability to CW input power levels. The development of high-power amplifiers, robust low-noise amplifiers and T/R switches on the same GaN monolithic process will bring to the next generation of fully-integrated T/R module front-end MMICs.

Index Terms – AESA systems, GaN MMIC, GaN SPDT switch, robust GaN LNA, T/R modules.

I. INTRODUCTION

Phased-array radar systems, based on active electronically scanned antennas (AESA) equipped by a huge number of Transmit/Receive (T/R) modules are on the leading edge of radar technology and are expected to play a key role in a variety of applications, from satellite communications and remote sensing, to surveillance and electronic warfare.

A typical T/R module is made up of a GaAs MMIC chipset, consisting in a high-power amplifier, a low-noise amplifier protected by a limiter, and a multi-functional chip, namely Core-Chip, to which the RF phase and amplitude control functions are ascribed [1-6]. In addition, a ferrite circulator routes the transmit (receive) signals from (to) the HPA (LNA) to (from) the antenna. However, the rising need for higher output power levels, broader bandwidth, higher operating voltages and higher robustness, as well as for more compact, reduced-weight modules, has been driving the technological advancement toward the development of alternative integrated circuit technologies. In particular, GaN monolithic technology is an excellent candidate for improving future front-end solutions [7], due to the inherent linearity and power handling capabilities of GaN HEMT devices.

The effectiveness of GaN for high power amplifiers design and fabrication is broadly accepted and demonstrated [8]; nevertheless, it can dramatically improve T/R module integration if it is considered for LNA and T/R switch design [9-11]. In fact, exploiting inherent GaN HEMTs ruggedness, robust low-noise amplifiers [12-20] can be designed avoiding the use of limiting circuits along the RX path. Moreover, the realization of GaN SPDTs able to handle high power levels leads to the possibility of swapping the ferrite circulator with an integrated circuits [21-29]. In prospect, a full integration of the T/R front-end in GaN technology, as depicted in Fig. 1, seems to be feasible in a near future, resulting in a noteworthy reduction of the overall T/R modules’ size, weight and costs.

Fig. 1 Block diagram of a T/R module front-end implementation in GaN technology.
In Section II, a GaN HEMT monolithic process developed by SELEX-ES is presented. Such technology has been adopted to design and realize a number of robust GaN MMIC T/R switches and low-noise amplifiers, that are described in Sections III and IV, respectively.

II. TECHNOLOGY

The MMICs discussed in this work have been fabricated with the SELEX-ES GaN-HEMT microstrip monolithic technology. The process is based on an epi-layer structure of GaN/AlGaN/GaN deposited on semi insulating SiC substrates by either MOCVD or MBE techniques. The mask levels for MMIC fabrication are based on a mix and match procedure utilizing both I-Line Stepper and Electron Beam Lithography for the fabrication of the high resolution quarter micron Gate dimensions necessary for the HEMT devices. After active device formation the MMIC fabrication process comprises: the deposition of NiCr thin-film resistors, MIM capacitors and electro-plated inductors and interconnect transmission lines, with air-bridges where necessary. The fabrication process is concluded with back-side wafer processing for the fabrication of through substrate via-hole interconnects. Further details on the complete fabrication process and the devices characterization and modeling can be found in [30]. This process is compatible with an innovative (patent pending) implementation of Field Plate to mitigate short-channel effects. In particular, a Schottky plate is placed between the gate and drain electrodes, and biased at a zero or positive (1 V) voltage through a 1 kΩ resistor. Further details can be found in [31].

Fig. 2 Microphotograph of the X-band SPDT switch.

A. Transmit/Receive SPDT

A well-designed T/R switch has to be featured by low insertion loss, high isolation, high linearity and high power handling. To meet such requirements, the X-Band single-pole double-throw switch is based on the standard series/shunt FET switch topology, where the key building block is represented by a resonated-type single-FET switch [28] adopted as a series element in conjunction with an optimized number of shunt elements.

As far as linearity and survivability are concerned, a very high power handling has been measured at 12 GHz, as shown in Fig. 3, where 39 dBm input power causes no noticeable compression phenomena, neither damage. Due to limited test bench power generation capabilities, the 1 dB input power compression has not been reached.

III. X-BAND GAN MMIC CHIPSET

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B. Low Noise Amplifier

The design goal was to obtain a robust LNA with performance appropriate to short- and mid-term evolution of X-band SAR systems, such as...
Cosmo 2nd Gen (CSG). In particular, a noise figure less than 2.5 dB as well as a linear gain higher than 25 dB were chosen as target values. Such specifications have already been achieved in [32].

The applied test process consisted in exposing biased MMICs to a calibrated CW input RF power at 9.6 GHz, with a duration of 1 s, and measuring the post-exposure gain (after the RF overdrive). Such measurement process was repeated by incrementally increasing of 1 dB the input RF drive up to about 43 dBm. Due to the limited dynamic range of the power sensor, the post-exposure gain was not measured in linear region but at a compression level of about 17 dB. Fig. 5 (top) shows the output power under stress condition, while Fig. 5 (bottom) depicts the post-stress gain. LNA circuits show no performance degradation with an input RF overdrive up to 41 dBm.

In the following, an improved version of the X-band LNA reported in [32] is presented. In this second-run realization, a fine tuning of the first-run LNA output matching network has been performed with the main goal of achieving a lower gain ripple over frequency, while, as for the first LNA version, a specific approach for optimum noise performance has been adopted [33].

Fig. 4 depicts the second-run LNA, whose size is 3×2.5 mm². Measurement results on the fabricated MMIC show a noise figure of about 2.2 dB at the optimum drain voltage $V_{DS} = 10$ V. Notice that the MMIC is designed as including the input and output bonding wires (length 600 μm, diameter 25 μm), therefore the actual noise figure is expected to be some tenths of dB less than measured on wafer. As to the transducer gain, that is over 25 dB with an associated ripple of ±0.5 dB, the effects of simulated bonding wires were added to measured S-parameters. In the same way, the measured input and output return losses are better than 10 dB and 15 dB, respectively.

The ruggedness of this LNA has been investigated under input overdrive conditions.
Such measured power level is a remarkable result in terms of power handling capability and to the authors’ knowledge the fabricated LNA exhibits a state-of-the-art survivability for X-band applications.

IV. BROADBAND GAN MMIC CHIPSET

A. Transmit/Receive SPDT

The wideband SPDT power switch is based on the same transistor topologies and models outlined for the X-band version above. In this case, the design goal was to achieve a 2–18 GHz switch with insertion loss better than 2 dB, isolation higher than 25 dB, and power handling at 1 dB compression (P1dB) greater than 5 W [23, 27].

The series/shunt circuit topology adopted consists in one series device cascaded to two shunt FETs. Similar to the X-band circuit, the wideband design was performed using the compensation concept [29]: in particular, a resistor has been added in series with the high-impedance transmission line to reduce the resonance quality factor. A micrograph of the fabricated wideband SPDT switch, with overall dimensions 2.0x1.7 mm², is illustrated in Fig. 6.

![Microphotograph of the 2-18 GHz SPDT switch.](image)

The measured insertion loss performance of the realized switch is about 2 dB, while better than 25 dB isolation has been achieved all over the 2-18 GHz bandwidth: such results are fully compliant with the design goals. Finally, the measured input and output matching levels are better than 10 dB.

Regarding linearity and survivability, this broadband SPDT exhibits comparable power handling with respect to the X-band realization. Also in this case, as shown in Fig. 7, measured results at 12 GHz demonstrates no signs of damage with input power levels up to 39 dBm, where the P1dB has been reached.

![Insertion loss and output power of the 2-18 GHz SPDT switch vs. input power at 12 GHz.](image)

B. Low Noise Amplifier

The design goal was to achieve a robust low-noise amplifier operating in the 2–18 GHz bandwidth, exhibiting noise and gain performance in line with the state-of-the-art and that could survive a CW input power in excess of 5 W.

In order to satisfy these requirements, a three-stage circuit configuration, with each stage consisting of a two-cell distributed amplifier (2-2-2 topology), was firstly adopted [19]. This approach is quite unusual in a low-noise distributed amplifier, where typically a large number of cells are considered for each travelling wave structure.
With the aim of improving gain and noise performance of [19], without sacrificing robustness, a novel scheme (6-3-3 topology) was specifically developed to allow the fulfillment of the conflicting specifications of low noise, high gain, high maximum frequency, and robust operation. In particular, a smaller gate periphery has been selected for the first distributed stage, to reduce noise figure, together with a larger number of cells for each stages to flatten the gain response over frequency. A microphotograph of the fabricated LNA, with overall dimensions $3.8 \times 2.9 \text{ mm}^2$, is illustrated in Fig. 8 [20].

Linear and nonlinear tests have been performed following the same procedures as for the previous LNAs. The measured gain exhibits an average value of 23.3 dB with a ripple of $\pm 0.8$ dB in the 1–20 GHz frequency range: such a flat gain response demonstrates the effectiveness of the design approach. A minimum noise figure of 3.3 dB resulted at 3 GHz, while the noise figure does not exceed 4.7 dB at 18 GHz. Finally, the measured input and output return losses are better than 8.5 dB.

The $P_{in} - P_{out}$ characteristic of this MMIC was measured at $f = 4.5$ GHz, where the input return loss is better than 15 dB. The broadband LNA was driven with a CW input power up to 40 dBm for approximately 5 min. As shown in Fig. 9, $P_{dB}$ is reached for an output power of 22 dBm (corresponding to 1 dBm input power) while the typical TOI is 29 dBm. For higher input levels the output power saturates to 26 dBm.

It is worthwhile stressing that such MMIC can withstand more than 10 W input drive with no signs of damage: indeed, the 40 dBm limitation was due only to the available instrumentation, not to DUT failures. Such input power level is the highest reported for multi-octave LNAs without performance degradation.

V. CONCLUSION

GaN monolithic technology could represent a relevant breakthrough for the next generation of T/R module front-ends. Exploiting GaN features, HPA, power T/R switch and robust LNA can be fully integrated onto the same chip. This contribution demonstrates the near-future effectiveness of such implementation by the design of several GaN MMIC robust SPDTs and LNAs fabricated in the same technological process, both with narrowband and broadband operation.

REFERENCES


