Novel Design of Compact Low Pass Filter using Defected Ground Structure

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***Abstract*-This paper presents a novel design method of low pass filter using defected ground structure (DGS) as *quasi-lumped* element. The design chart is presented for design of quasi-lumped DGS inductors and a systematic design process is presented for design of higher pole DGS based LPF. Accuracy of the method is demonstrated by the design, simulation and testing of two fabricated LPF.**

***Index Terms* — Defected Ground Structure (DGS), Microstrip, Low pass Filter (LPF).**

I. INTRODUCTION

Emerging applications such as wireless communications continue to challenge RF/Microwave filters design with ever more stringent requirements-high performance, smaller size, lightweight, and lower cost. Design of low pass filters (LPF) using the defected ground structures (DGS) on microstrip line has been discussed by several authors [1]-[3]. Several shapes and arrangements of DGS slots are used. The DGS structure offers a *quasi-lumped inductive* element. This structure is used to replace the high impedance narrow microstrip line that is normally used as an inductor in the design of a high-low impedance low-pass filter (LPF) [4]-[6]. Very narrow width microstrip line section is inconvenient for fabrication and it also increases the length of a LPF. The DGS acts as an inductor and it reduces length of the LPF.

The DGS are normally used to get a 3-pole LPF and its specified characteristics are obtained through trial and error process on an EM-simulator. There is no systematic process to design a DGS based LPF either using the Butterworth response or the Chebyshev response.

This paper presents a systematic process to design a higher order Chebysev LPF using the DGS. The design specification of a given LPF is realized without any trial and error and final LPF is tested on the EM-simulator. The trial and error process on an EM-simulator for developing a higher order DGS based LPF is a very difficult and time consuming. The present method is novel in two aspects. At first we have characterized the DGS slot as *quasi-lumped* inductor operating at frequency below its resonant pole frequency. Secondly we have adopted systematically Chebyshev filter synthesis method to design the DGS based LPF. We present a design chart that correlates the DGS slot-head area to the quasi-lumped inductance and also to the inductive reactance at the cut-off frequency of the LPF. The design chart is extracted from the S-parameter response of the DGS on an EM-simulator. The synthesis method of the DGS based LPF follows the standard filter synthesis method [4]. The process is also applicable to the DGS based LPF with Butterworth response.

In order to validate the design method, we have designed two DGS based low- pass filters from the given specifications. We have also fabricated and finally tested both the filters on the Network Analyzer. The measured responses show good agreement with the simulation results.

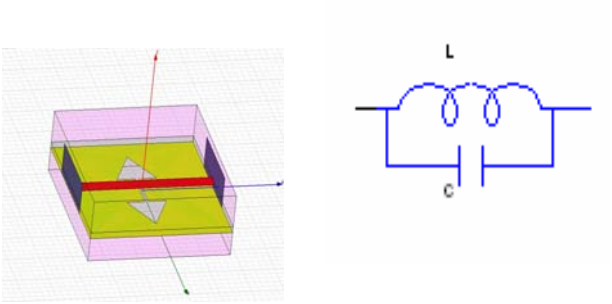
II. CHARACTERIZATION OF DGS BASED QUASI-LUMPED INDUCTOR

The triangle headed DGS slot is adopted in our design as it gives sharper cut-off as compared to the square headed and circle headed DGS [3]. The sharpness of cut-off of DGS slot appears as sharper cut-off of the LPF.

The triangle headed DGS slot shown in Fig.1 (a) is constructed in the ground plane of a 50Ω-microstrip line on the FR-4 substrate ($\varepsilon_r = 4.4$) with thickness $h = 0.8\text{mm}$. Its LC equivalent circuit is shown in Fig.1 (b). The inductance and capacitance of the DGS slot are computed from the equations given below [3]

$$C = \frac{5 f_c}{\pi\left(f_0^2 - f_c^2\right)} pF \quad (1)$$

$$L = \frac{250}{C(\pi f_0)^2} nH \quad (2)$$

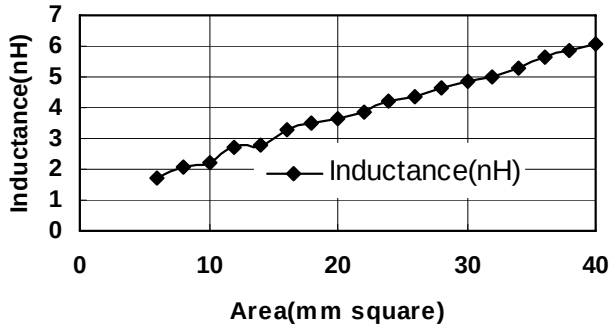


(a) (b)

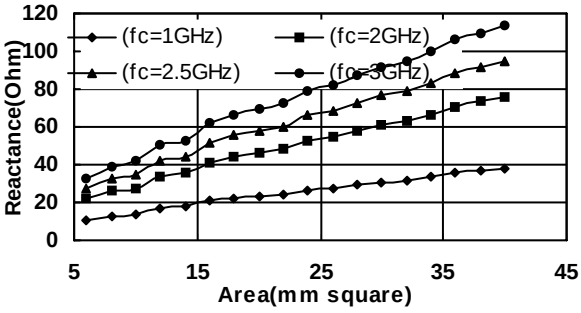
Fig. 1 (a) DGS in ground plane, (b) Equivalent Circuit

where f_c is the 3 dB cut-off frequency and f_0 is the pole frequency of the parallel resonance exhibited by the DGS slot .The inductance and capacitance for the variable area of a triangular DGS slot are obtained using above equations. We have taken slot area between 6 mm^2 to 40mm^2. Below the pole frequency f_0, the parallel resonance circuit behaves as an inductor. Therefore, the DGS slot behaves as a *quasi-lumped inductor* below the pole frequency f_0. The quasi-lumped inductor is frequency dependent. However at frequency up to cut-off frequency, the frequency dependence is small that can be ignored. For a given substrate i.e. for a specified relative permittivity and substrate thickness, the quasi-lumped inductance realized by the DGS depends only on the slot area of a DGS.

The inductance and inductive reactance of the DGS slot is plotted in Fig.2a and in Fig.2b respectively with respect to the slot head area. In case of the reactance, cut-off frequency f_c is a parameter. In order to extract the inductance and capacitance of a DGS from the S-parameter response on an EM-simulator, we have used 50 ohm microstrip line with triangular slot DGS. The separation between slot-head is maintained at l = 4.74 mm and coupling slot gap width g =0.5mm for all sizes of slot-heads. The inductive reactance chart shown in Fig.2 is used to design the low-pass filter using DGS. It is used to find the slot area of equivalent reactance at the cut-off frequency of the LPF. The DGS capacitance is not important in the proposed design method as below resonant pole frequency the DGS behaves effectively as an inductor. However, the slot length connecting two DGS slot-heads offers some inductive discontinuity to the microstrip. It could be accounted for by reducing the size of the DGS slot-heads.



(a); Inductance (nH) versus slot area

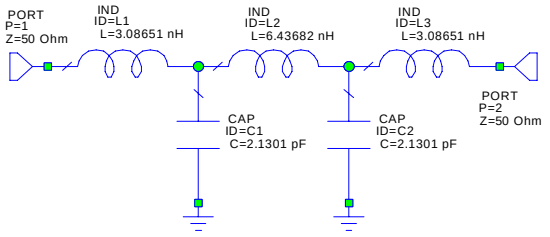


(b): Inductive reactance versus slot - area

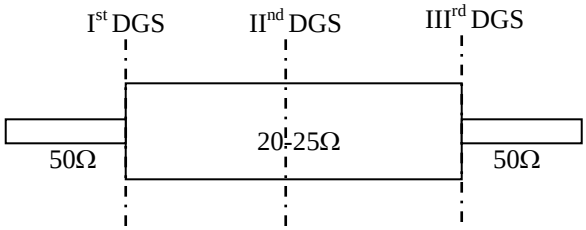
Fig. 2: Design Chart of DGS based quasi-lumped inductor

III. NOVEL DESIGN PROCESS

The present design method is based on the prototype of Chebyshev type low-pass filter design. Usually component values of such filter are obtained from the ripple factor in pass-band and order of i.e. the number of poles of a filter. The normalized component values i.e. g- values of the components are tabulated at the pass-band ripple edge frequency f_r [5]. The 3 dB cut-off frequency f_c is not meaningful in the design of a lumped element based Chebyshev type LPF. However, in case of a LPF based on microstrip with DGS, this design process is not suitable. Because it is difficult to achieve low loss i.e. small ripple factor such as 0.01 dB for the DGS based LPF. The microstrip line and the DGS slot both are lossy components. Therefore, we prefer to design the DGS based LPF at 3 dB cut-off frequency f_c. However, as the g-values of the Chebyshev type LPF are given only at the pass-band ripple edge frequency f_r, we have to translate the given cut-off frequency f_c to the corresponding ripple edge frequency f_r. For a given number of poles and the ripple factor in the pass-band there is definite ratio of two frequencies [5]. We have demonstrated the design process for a 5-pole Chebyshev LPF. Its equivalent lumped circuit is shown in Fig.3a.



(a): Lumped element LPF



(b): Locations of DGS slots on microstrip in the DGS based 5-poles LPF.

Fig.3: Schematic diagram of 5-pole LPF.

Design steps:

i. Prototype normalized lumped element values i.e. the g-values of a Chebyshev type LPF are given at its edge frequency f_r. In the present design process, the ripple edge frequency f_r is determined from the given 3 dB cut-off frequency f_c and the ripple factor of the LPF. The renormalized lumped elements are determined at the ripple edge frequency f_r [4,5].

ii. The low impedance microstrip line sections are used to realize the lumped capacitors. The following expression is used for this purpose [4.6]

$$l_c = \frac{\lambda_{gr}}{2\pi}\sin^{-1}\left(\omega_r C Z_{oc}\right) \qquad (4)$$

Where l_c is length of microstrip section to realize the lumped capacitance C, Z_{oc} is the characteristic impedance of the microstrip. It could be in the range 20 Ω -25 Ω. $\omega_r = 2\pi f_r$ and λ_{gr} is the guided wave length of microstrip at f_r. The lengths of all microstrip sections corresponding to all lumped capacitors are combined to form one continuous microstrip section. It is fed by and terminated into 50 Ω microstrips.

iii. The DGS as quasi-lumped inductors are used to realize the lumped inductors. The design charts shown in Fig.2 are used to compute the area of the DGS slots corresponding to the lumped inductor at f_r. The charts of Fig.2 are valid for the FR-4 substrate with thickness h=0.8mm. For other substrate, a designer should prepare such charts using any EM-simulator. This process is discussed in section-II.

The first DGS slot corresponding to the first series inductor shown in Fig.3 is located at the junction of 50 Ω microstrip line and low impedance microstrip line. The low impedance microstrip line (20-25 Ω) corresponds to the lumped capacitor. The second DGS slot corresponding to the second lumped inductor is located at the end of line length on low impedance microstrip section that corresponds to the first lumped capacitor. The locations of other

DGS slots on the microstrip line follow the similar scheme. For a 5-pole DGS based LPF the locations of DGS slots are illustrated in Fig.3b.

iv. At this stage layout of the DGS based LPF is ready. Using the EM-simulator, we can optimize the size of DGS to achieve the design objective. The size of DGS slots are reduced by a small value to account for the inductive discontinuity. The size of DGS heads is reduced to maintain specified 3 dB cut-off frequency.

v. The optimized DGS based LPF is fabricated and its performance is measured on a Network Analyzer. The dimensions of the fabricated LPF are also measured carefully on a traveling microscope. The LPF with its measured dimensions is again simulated on the EM-simulator to compare its performance against the measured results. The deviation in the dimensions of the designed and fabricated LPF and its impact on the performance of a LPF helps us to characterize the fabrication process. The deviation in the fabricated and designed dimensions could be taken into account at the design stage itself in order to get specified response of a LPF.

IV. LPF DESIGN EXAMPLES

We present design, simulation and measurement of two 5-pole DGS based LPF. The lumped element prototype is shown in Fig. 3a and locations of DGS slots are shown in Fig.3b. The specifications for the 5-poles LPF are given below

a. The first DGS based filter is designed at 2.5 GHz that is the 3dB cut off frequency (f_c). The pass-band ripple factor (IL) is 0.01dB.

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b. The second LPF has IL= 0.01dB. Its cut-off frequency is 1.0 GHz.

For a 5-pole LPF with 0.01 dB ripple factor, the ratio of cut-off frequency and ripple band edge frequency is f_c/f_r= 1.292 . Therefore, ripple band edge frequency f_r for the first LPF is 1.95 GHz; whereas for the second LPF it is 0.78 GHz.

Table-1: Parameters of the designed LPF at f_c=2.50GHz

	L_1	L_2	L_3	C_1	C_2
Prototype g-value	0.756	1.577	0.756	1.305	1.305
Lumped Value	3.087 (nH)	6.437 (nH)	3.087 (nH)	2.130 (pF)	2.130 (pF)
Capacitive line length	-	-	-	7.5 mm	7.5 mm
Capacitive line width	-	-	-	4.74 mm	4.74 mm
Fabricated capacitive line width	-	-	-	4.79 mm	4.79 mm
DGS slot dimensions	10 mm^2	30 mm^2	10 mm^2	7.5mm	7.5mm
Optimized LPF dimensions	8 mm^2	28 mm^2	8 mm^2	7.5mm	7.5mm
Fabricated dimensions	8.5 mm^2	29 mm^2	8.5 mm^2	7.83mm	7.83mm

Table-2: Parameters of designed LPF at f_c=1.0GHz

	L_1	L_2	L_3	C_1	C_2
Prototype g-value	0.756	1.577	0.756	1.305	1.305
Lumped Value	7.696 (nH)	16.050 (nH)	7.696 (nH)	5..311 (pF)	5..311 (pF)
Capacitive line length	-	-	-	16 mm	16 mm
Capacitive line width	-	-	-	4.74 mm	4.74 mm
Fabricated capacitive line width	-	-	-	4.66 mm	4.66 mm
DGS slot dimensions	44 mm^2	92 mm^2	44 mm^2	16 mm	16 mm
Optimized LPF dimensions	43.3 mm^2	92 mm^2	43.3 mm^2	16 mm	16 mm
Fabricated dimensions	44 mm^2	91 mm^2	44 mm^2	15.7 mm	15.7 mm

Following the design steps discussed in section-III; the g-values, lumped elements, initial DGS size, optimized dimensions and fabricated dimensions for both filters at the ripple band edge frequency f_r frequency 1.95 GHz (f_c=2.50) GHz and 0.78 GHz (f_c=1.0)are summarized in table-1 and table-2 respectively. The components values for f_c=2.50 GHz LPF are also shown in the circuit diagram of Fig.3a.

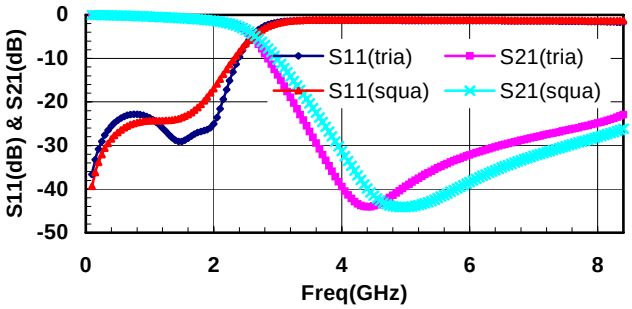


Fig.4: Response of LPF with square and triangular slots DGS

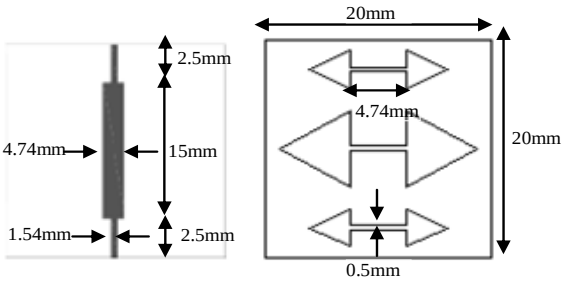


Fig. 5: Layout of the LPF (a) Top side, (b) Bottom side

Fig. 6: Fabricated LPF (a) Top side, (b) Bottom side

In order to verify effectiveness of the triangle headed DGS, we have simulated the first LPF on an EM-simulator by using both the square and triangular DGS slots of same area. Fig.4 shows that the 3 dB cut-off for both cases is 2.5 GHz. However, sharpness of the cut-off of a LPF with the triangular DGS slots is better than the sharpness offered by the square DGS slot. Therefore, in the present design, we have adopted the triangular slot DGS. The layout of the designed LPF at f_c=2.5 GHz is shown in Fig.5 and the fabricated filter is shown in Fig.6.

Fig.7 shows the simulated and experimental S-parameter response of 2.5 GHz LPF. The 20 dB rejection is above 8 GHz that is the measurement range of our Scalar Network Analyzer. The simulation is done for the optimized dimensions of LPF that is used for the fabrication. We also measured the actual dimensions of the fabricated LPF shown in table-1. We again simulated the LPF for its fabricated dimensions. Fig.7 compares both the simulations against the measured results. The dimensions of fabricated LPF do not have significant effect on the response of a LPF in the pass-band. However, in the stop-band measured response shows better agreement with the simulation done with actual dimensions of the fabricated LPF. The EM simulations do not account for the presence of the connectors and their soldering. This is could be the reason for deviation of simulated results from the measured one. Table-3 compares the performance in more details. The insertion loss in pass-band up to the ripple band edge frequency is within 1 dB. There is only 0.02 GHz change in the simulation and measured frequency. However, 0.15 GHz deviation from the specification is due to deviation in the fabrication of LPF. Therefore, if we design our LPF at 2.65 GHz, we may get 3 dB cut-off frequency near to 2.5 GHz.

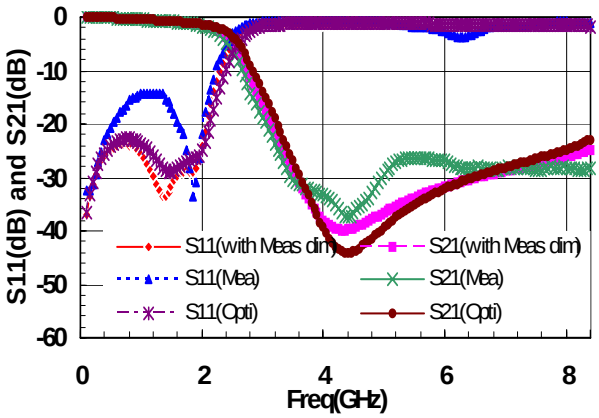


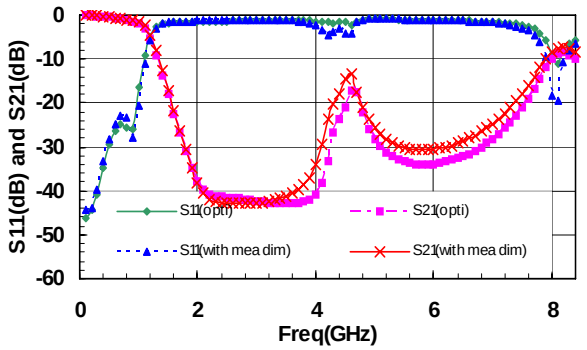
Fig. 7: Simulated response- (i) optimized design, (ii) fabricated dimensions and measured response of LPF with 2.5 GHz cut-off frequency

Similarly Fig. 8a shows results of two simulations of 1 GHz LPF – one for its dimensions of optimum design and another for the dimensions of fabricated

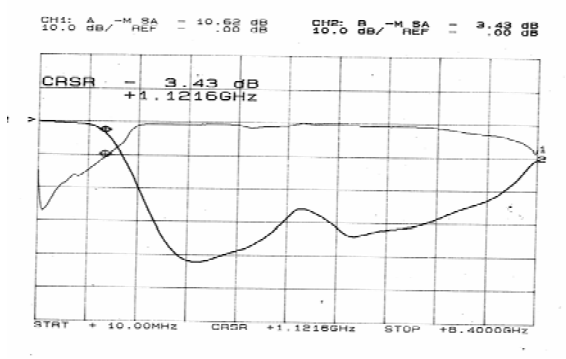
Table-3: LPF-I at fc=2.5 GHz

LPF	IL 0-2 GHz	f_{3dB} (GHz)	f_{pole} (GHz)	Sharpness GHz /dB
Simulation Optimized design	0.89	2.47	4.41	0.77
Simulation Measured dimension	0.89	2.37	4.28	0.74
Measured result	0.97	2.35	4.45	0.75

LPF. The experimental performance of this LPF is shown in Fig.8b. Table-4 shows the detailed comparison of the simulated performances of the 1 GHz LPF against the measured results. The optimization is done at cut-off frequency 1.15 GHz instead of given specification 1.00 GHz. So the fabricated LPF has f_c 1.12 i.e. 0.03 GHz less. Again we can improve our design we take in to account expected decrease in frequency in the present fabrication process at the design stage itself. The insertion loss in pass-band is 0.8 dB cut-off frequency.



(a): Simulated response- designed dimensions and fabricated dimensions



(b) Measured dimensions of LPF.

Fig. 8: Simulated and measured response of LPF at 1GHz

Table-4: Table-4: LPF-II at fc=1.0 GHz

LPF	IL 0-0.7 GHz	f_{3dB} (GHz)	f_{pole} (GHz)	Sharp-ness GHz/dB	Spurious Freq (GHz)
Simulation Optimized design	0.82	1.15	2.95	0.41	4.7
Simulation Measured dimension	0.82	1.13	2.94	0.42	4.58
Measured result	0.80	1.12	2.822	0.52	4.56

V.CONCLUSION

We have presented a systematic design process to design the Chebyshev type 5 pole low –pass filter using the DGS as a quasi-lumped inductor. Accuracy of the design is demonstrated by the design of two LPF.

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